PERSONAL INFORMATION

VALERIU BEIU

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PERSONAL STATEMENT

I like to take abstract concepts for difficult but practical applications, turn them into efficient algorithms, and then design innovative VLSI circuits performing them optimally (e.g., at ultra-high speeds, with very low power/energy, highly reliable, etc.). I am extremely interested by emerging nanoelectronics and in particular by bio-/brain-inspired nano-architectures (massively parallel, adaptive/reconfigurable, fault-tolerant, using alternate communication schemes), and by their optimized designs inspired by arrays (e.g., biological/ion-channels, cellular, systolic).

My current research activities are focused on nano-architectures, my major aim being to strengthen cooperation on bio-/brain-inspired nano-architectures, promote education, and generate new funding opportunities. This endeavour is based on a wide international cooperation, as quite a large number of researchers are actively pursuing nano-architectural initiatives. My hope is that, through direct collaboration (special sessions, visits, grants, etc.), the number of experts joining such efforts will grow. The ultimate goal is to advance understanding of enabling architectures matching the novel nano-devices and associated communication schemes, performing research starting from ultra-low power reliability-enhanced bio-/brain-inspired circuitry up to large scale systems.

SPECIALIZATION

- Bio-/brain-inspired nano-architectures, i.e., fault-tolerant & low-power
- VLSI (ultra-low power, reliability enhanced gates/circuits/systems, novel communication schemes)
- Digital design (including threshold logic)
- Circuit and VLSI complexity
- Hardware implementations of neural networks (including constructive neural learning)
- Biological / neural computations and communication (including massively parallel architectures)
- Computer architectures and computer arithmetic

EXPERIENCE

- Involved in research for 36 years
- Holding management positions for over 20 years
- In executive positions for more than 10 years

EXPERTISE

My expertise encompasses a range of areas starting from circuit/VLSI complexity, going through information theory, optimization techniques, and neural computations, to advanced VLSI/nanoelectronics and adaptive/reconfigurable circuits and systems

Besides research, I have been teaching/lecturing since 1981. Between 1981 and 1983 I have been teaching part time, while since 1983 I have been teaching full time in the Computer Science & Engineering (CSE) Department of the University “Politehnica” of Bucharest (UPB): Assistant Professor (1983–1990), Senior Lecturer (1990–1995), and Associate Professor (1995–2001). Between 1984 and 1991 I supervised 29 MSc candidates. Between 2001 and 2005, I was with the School of Electrical Engineering & Computer Science (EECS), Washington State University (WSU), where I supervised two MSc and one PhD, and contributed to getting the ABET accreditation of the newly founded Computer Engineering program. In 2005 I joined the College of Information Technology (CIT), United Arab Emirates University (UAEU) and I also became visiting professor with the University of Ulster (UU). At UAEU I contributed to the ABET accreditation of the CIT, which started offering MSc programs in Fall 2013. That is why, since joining UAEU (in 2005), my graduate supervision has been limited to: invitations on 8 PhD evaluation committees, co-supervising 2 MSc, and advising 1 PostDoc, while since Fall 2015 I have started teaching in two of the graduate programs of the “Aurel Vlaicu” University of Arad (UAV). Additionally, I was invited to give 17 tutorials and 44 seminars/lectures.

BIO-SKETCH

I graduated in 1980 from the Computer Science & Engineering Department of the University "Politehnica" of Bucharest (Romania) with a MSc thesis on high-speed graphic workstations (Best MSc Thesis Award). I researched, designed and developed ultra high-speed floating-point units (FPUs) and central processing units (CPUs) for two years while with the Research Institute for Computer Techniques, Bucharest (Romania). Returning to the University "Politehnica" of Bucharest, I became Assistant Professor (1983), Senior Lecturer (1990), and Associate Professor (1995), teaching, researching (computer architecture, VLSI design, digital circuits, artificial neural networks), and supervising (29 MSc theses).

In 1991, being awarded both a Fulbright Research Fellowship (USA) and a PhD Scholarship (Belgium), I went for the doctoral studies, and have been on leave of absence from the University "Politehnica" of Bucharest (till 2001).

- 11/1991 – 11/1994 ▪ PhD candidate with the Electrical Engineering Department, Katholieke Universiteit Leuven (Belgium), where in May 1994 I earned my PhD summa cum laude (highest honours) for a thesis on area- and time-efficient VLSI implementations of artificial neural networks using threshold logic gates.
- 12/1994 – 09/1996 ▪ Human Capital and Mobility Individual Research Fellow of the European Union with the Centre for Neural Networks, King's College London (UK), conducting research on programmable neural arrays.
- 10/1996 – 08/1998 ▪ Director's Postdoctoral Fellow with the Space and Atmospheric Sciences Division, Los Alamos National Laboratory (USA), investigating adaptive / reconfigurable field programmable neural arrays for deployable adaptive processing systems.
- 09/1998 – 05/2001 • CTO and co-founder of RN2R LLC and Fellow of Rose Research (Dallas, USA), coordinating research on ultra-fast low-power VLSI enabling neural-inspired gates and circuits.

From June 2001 I became an Associate Professor with the School of Electrical Engineering and Computer Science, Washington State University, involved in teaching (advanced VLSI/ nanoelectronics, ASICs/FPGAs, neural computations, computer architecture), researching (low-power and highly reliable VLSI circuits, emerging biological-inspired nano-architectures), and supervising (1 PhD and 2 MSc theses). In March 2005 I was offered a visiting professor position with the School of Intelligent Systems, University of Ulster (Londonderry, UK), and in July 2005 I joined the College of Information Technology (CIT), United Arab Emirates University (UAEU, Al Ain, UAE) as Chair of Computer Engineering (2005–2006), where in 2006 I was promoted to Associate Dean for Research & Graduate Studies (2006–2011). Since August 2015 I joined "Aurel Vlaicu" University of Arad (UAV, Arad, Romania), while still having on-going research grants with UAEU.

I am/was PI on 28 grants/contracts, co-PI on 16 others, as well as PI on 93 short-term travel grants, all of these totalling over 51 M$. The research results have been published or accepted for publication: 2 books (3 more in progress), 8 book chapters (7 invited, and 5 more in progress), 11 patents (1 more in progress), 28 journal papers (2 invited, and 5 more in progress), and over 190 conference papers (26 invited and 6 best paper awards); as well as presented over 380 times (out of which 190 invited keynote/tutorials/ presentations) and cited over 1200 times (excluding self-citations).

I have been a reviewer for the National Science Foundation (USA), the European Commission (EU), as well as for the science foundations of Belgium, Cyprus, Switzerland, UAE, as well as for many journals and conferences. I was an Associate Editor of the IEEE Transactions on Neural Networks (2005–2008) and of the IEEE Transactions on VLSI Systems (2011–2015), and I am an Associate Editor of the Nano Communication Networks (since 2010). I have contributed to organizing 109 international conferences and 10 invited workshops/sessions, chaired 56 conference sessions, and I am a Senior Member of the IEEE since 1996 (in 1997 I was the Program Chairman of the IEEE Los Alamos Section), a founding member of the European Neural Network Society (ENNS), and a member of: the Association for Computing Machinery (ACM), the International Neural Network Society (INNS), the EU Marie Curie Fellowship Association (MCFA), and the American Nano Society (ANS). Additionally, I am a member of the SRC-NNI Working Group on Novel Nano-architectures (since 2003), the IEEE CS Task Force on Nano-architectures (since 2005), and the IEEE Emerging Technologies Group on Nanoscale Communications (since 2010).

WORK EXPERIENCE

Sept. 2015 – Present

Professor Higher education

"Aurel Vlaicu" University of Arad (UAV), Faculties of Exact Sciences and Engineering
Complex M, Str. Elena Dragoi nr. 2-4, 310330 Arad, Romania

- Research on "Novel Bio-inspired Cellular Nano-Architectures" (PI on a research grant entitled BioCell-NanoART, POC-A1-A1.1.3-E-2015)
- Teaching (graduate level) "Nano-Bio Fundamentals," "Neural Computations," and "Intelligent Circuits"

Sept. 2008 – Aug. 2015

Professor Higher education

United Arab Emirates University (UAEU), College of Information Technology
Maqam Campus, Bldg. E1, PO Box 15551, Al Ain, UAE

- Research and instruction in the areas of designing with nanometer-scale CMOS devices, novel (beyond CMOS) devices
- Particular focus on brain-inspired hierarchical optimal interconnect topologies/networks, novel array-based redundancy schemes (e.g., axon-inspired)
- Investigating alternate communication paradigms for CMOS and beyond CMOS
- Enabling (patentable) statistical optimizations for advanced CMOS circuits

Sept. 2006 – Aug. 2011

Associate Dean for Research and Graduate Studies Higher education

United Arab Emirates University (UAEU), College of Information Technology
Maqam Campus, Bldg. E1, PO Box 15551, Al Ain, UAE

- In charge of the research development of the College of IT, providing administration support to faculty
- Facilitated multi-disciplinary research initiatives, collaborations with international universities, and college development
- Provided support to faculty for grant proposals and submission opportunities
- Responsible for overseeing significant labs developments, setting new directions, and actively contributed to securing industrial support (grants, equipment, service, and gifts/donations)
- Liaison between faculty and industry
- Have established a PhD program as well as 4 new MSc programs
- From 2006 to 2011, CIT research funding has increased 10×, the number of publications 4×, and the number of citations 3×
- Research and instruction related to nano-architectures

Sept. 2005 – Aug. 2006

Chair Computer Engineering Higher education

United Arab Emirates University (UAEU), College of Information Technology
Al Jimi 1, PO Box 17555, Al Ain, UAE

- Responsible for the CE program, operations, strategic growth and relationships
- Oversee academic personnel actions
- Teaching VLSI design and computer architecture and doing research on nano-architectures

Jun. 2001 – Aug. 2005

Associate Professor Higher education

Washington State University (WSU), School of Electrical Engineering and Computer Science
Spokane 102, Pullman, WA 99164, USA

- Teaching advanced VLSI/nanoelectronics, ASICs/FPGAs, neural computations, computer architecture
- Research on low-power and highly reliable VLSI circuits, emerging biological-inspired nano-architectures
- Supervising 1 PhD and 2 MSc
- Worked among others on Direct Digital Frequency Synthesizers (DDFSs) for reconfigurable communication systems, and on ultra-low power sub-threshold circuits using an original cross-coupled adaptive body biasing scheme for boosting reliability

Sept. 1998 – May. 2001 **Chief Technical Officer / Fellow (co-founder)** Industry / Research
RN2R / Rose Research LLC
14850 Monfort Drv., Dallas, TX 75240, USA
- Coordinating and doing research on ultra-fast low-power VLSI enabling neural-inspired gates and circuits
- Pioneered FastLogic, an enabling VLSI technology based on novel ultra-fast logic gates, and a systematic design methodology for using them (several versions of FastLogic gates have been designed, simulated, tested, and patented)
- Low-power was achieved by means of a novel self-timed power-down mechanisms, as well as differential (charge recycling) circuits
- Investigated potential applications like, addition, multiplication, multiply-accumulate, en/decryption (for crypto-processors), and graphic accelerators

Oct. 1996 – Aug. 1998 **Director's Postdoctoral Fellow** Research
Los Alamos National Laboratory (LANL), NIS Division
MS D466, Los Alamos, NM 87545, USA
- Investigated adaptive/reconfigurable field programmable neural arrays (FPNAs) for deployable adaptive processing systems (DAPS)

Dec. 1994 – Sept. 1996 **EU HCM Individual Research Fellow** Higher education
King's College London, Mathematics / Centre for Neural Networks
Strand, London, WC2R 2LS, UK
- Conducted research on programmable neural arrays (PNAs)

Nov. 1991 – Nov. 1994 **PhD candidate on Doctoral Scholarship (Research Fellow from 06.1994)** Higher education
Katholieke Universiteit Leuven, ESAT-ACCA
Kasteelpark Arenberg 10, Leuven, B-3001 Belgium
- Researching on hardware/VLSI implementations of threshold logic gates (perceptrons)
- Improved the size/depth complexity for certain classes of Boolean functions and found novel VLSI-friendly constructive (learning) algorithms

Apr. 1990 – Aug. 1991 **Co-founder and President** Industry
Spring Software Consult SRL
Blvd. Magheru 20, Bucharest, RO-10721 Romania
- Negotiated, won, managed, and coordinated contracts on en/decryption, CAD training, software package for microbusiness, and a data acquisition CAD tool

Jan. 1990 – Jun. 2001 **Senior Lecturer ("on leave of absence" from 09.1991)** Higher education
University "Politehnica" of Bucharest, CSE Department
Spl. Independentei 313, Bucharest, RO-10334 Romania
- Research and instruction in the areas of computer architecture, VLSI design, digital circuits, and artificial neural networks (continuing the activities started while an Assistant Professor)

Jan. 1983 – Jan. 1990 **Assistant Professor** Higher education
University "Politehnica" of Bucharest
Spl. Independentei 313, Bucharest, RO-10334 Romania
- Research and instruction in the areas of computer architecture, VLSI design, digital circuits, and artificial neural networks (publishing about their capabilities and delving into Boltzmann machines), and supervising (29 MSc theses)
- Early focus on smart memories (e.g., content addressable, set processing, hierarchical, self-testable) and regular arrays (e.g., systolic, cellular) for dedicated tasks (e.g., antialiasing), as well as watch-dog systems

Sept. 1981 – Jan. 1983 **Senior Researcher** Industry / Research
Research Institute for Computer Techniques
Cl. Floreasca 167, Bucharest, RO-14459 Romania
- Researching on digital VLSI, and in particular on accelerating arithmetic logic units (ALUs) using new and enhanced algorithms with innovations at the microprogramming level
- Patented a mutual exclusion circuit

Sept. 1980 – Aug. 1981 **Research Engineer** Industry / Research
Research Institute for Computer Techniques
Cl. Floreasca 167, Bucharest, RO-14459 Romania
- Involved in the testing of the CE-100 computer (PDP)
- Designed ultra high-speed floating-point units (FPUs) and central processing units (CPUs)

Visiting Positions **Visiting Professor** Research

▪ Mar. 2005 – Aug. 2011	University of Ulster	UK
▪ Apr. 2008	Los Alamos National Laboratory	USA
▪ Aug 2004	Heinz Nixdorf Institute	Germany
▪ Jul. 2003	Heinz Nixdorf Institute	Germany
▪ Jul. 2002	Los Alamos National Laboratory	USA

EDUCATION AND TRAINING

Sept. 1996 – Aug. 1998 **Postdoctoral LANL Director's Fellow** EQF level 8
Los Alamos National Laboratory (USA)
- Investigated adaptive/reconfigurable field programmable neural arrays for deployable adaptive processing systems (hardware implementations of neural networks)

Oct. 1994 – Aug. 1996 **Postdoctoral EU Human Capital and Mobility Fellow** EQF level 8
King's College London (UK)
- Leading research on programmable neural arrays (hardware implementations of neural networks)

Oct. 1991 – Sept. 1994 **PhD in Electrical Engineering (Scholarship)** **Summa cum laude** EQF level 8
Katholieke Universiteit Leuven (Belgium)
- Thesis title "Neural Networks Using Threshold Gates — A Complexity Analysis of Their Area- and Time-Efficient VLSI Implementations"
- Improved on the size/depth complexity for certain classes of Boolean functions
- Found novel VLSI-friendly constructive (learning) algorithms (EDA-like synthesis)

Sept. 1992 **Specialization (Scholarship)** EQF level 7
Institut Universitaire Kurt Bösch (Switzerland)
- Neural Networks

May 1989 – Sept. 1991 **PhD candidate in Computer Engineering** EQF level 7
University "Politehnica" Bucharest (Romania)

▪ 1989: PhD entrance exam "VLSI Efficient Implementations of Parallel Architectures"	10/10
▪ 1990: PhD exam "Mathematical Complements"	10/10
▪ 1990: PhD exam "Systolic and Neural Architectures"	10/10
▪ 1990: PhD exam "Novel VLSI Structures"	10/10
▪ 1991: PhD exam "Parallel and Advanced Architectures"	10/10

Jan. 1980 – June.1980 **Master of Science in Computer Engineering** **Best MSc Award** EQF level 7
University "Politehnica" Bucharest (Romania)
- Thesis title "High-Speed Graphic Parallel Accelerators"

Sept. 1975 – Dec. 1979 **Bachelor of Science in Computer Engineering** **4th place (9.76/10)** EQF level 6
University "Politehnica" Bucharest (Romania)
- Graduated from the CSE Department of the Faculty of Automatic Control and Computer Science

Sept. 1971 – Jun. 1975 **Baccalaureate** **1st place (9.26/10)** EQF level 5 & 6
National College of Computer Science "Tudor Vianu"
- The Diploma of Baccalaureate states that I am a *"programmer and software assistant analyst."*

Alma maters

University "Politehnica" Bucharest	Founded in 1818, it is the largest technical university of Romania with over 28,000 students (www.upb.ro/en/). The Department of Computer Science & Engineering (CSE) was founded in 1969 (cs.pub.ro/) by Prof. Mircea Petrescu.
Katholieke Universiteit Leuven	Founded in 1425, it is the oldest catholic university of Northern Europe, recognized for names like Erasmus, Mercator, and Vesalius (www.kuleuven.be/english/), is *in the world's top 100 universities* (**35** in the THE World University Rankings 2015-2016), and is the largest university in Belgium. The EE Department of was founded in 1900 (www.esat.kuleuven.be/index.en.php).
King's College London	Founded in 1829, is one of the larger and oldest of London (www.kcl.ac.uk), with about 23,000 students, and is *in the world's top 100 universities* (**27** in the THE World University Rankings 2015-2016). The Mathematics Department (www.kcl.ac.uk/nms/depts/mathematics/) has received the highest rating in the Research Assessment Exercise, being a 'center of excellence'. *The Centre for Neural Networks* was the coordinator of the *European Neural Networks Network of Excellence*.

Supervisors

Prof. Mircea Petrescu	Founder of the CSE Department, Vice-Provost, and Director of the Computer Center, State Secretary of the Government of Romania, as well as Visiting Professor at the University of California at Berkeley (USA) and at the University of Grenoble (France). He was Vice-President of the Romanian Academy of Technical Sciences and is an honorary member of the Romania Academy of Sciences. He has published more than 120 articles and 8 books. http://ro.wikipedia.org/wiki/Mircea_Petrescu
Prof. Joos Vandewalle	Has been Vice-Dean, Visiting Professor at the University of California at Berkeley (USA), Chairman of the EE Department, and holder of the Francqui Chair on Neural Networks at the Universite de Liege (Belgium). He was elected Fellow IEEE in 1992, and Fellow IEE in 1998, and was the Vice-President for Region 8 of the IEEE Society on Circuits & Systems. He has published over 600 articles and 18 books. http://www.esat.kuleuven.be/stadius/person.php?persid=18
Prof. John G. Taylor	Has been Director of the Centre for Neural Networks and President of the International Neural Network Society. He has held positions at the Institute of Advanced Study, Princeton (USA), Institut des Hautes Etudes, Paris (France), Christ College, Cambridge (UK), Mathematics Institute, Oxford (UK), Physics Department, Southampton (UK), Queen Mary College, London (UK), Rutgers University, New Jersey (USA). He has published more than 400 articles and over 20 books. http://en.wikipedia.org/wiki/John_G._Taylor

PERSONAL SKILLS

Mother tongue(s): Romanian

Other language(s)

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken interaction	Spoken production	
English	C2	C2	C2	C2	C2
	Took English in school (1967-1975) as well as in university (1975-1977) Lived and worked in UK (1994-1996), USA (1996-2005), and UAE (2005-2015)				
French	C2	C2	C2	C2	B2
	Started learning when 3 years old; took French in school (1971-1975); lived and worked in Belgium (1991-1994)				
Italian	B1	B2	A2	A2	A1
	No formal training (have watched Italian TV; Italian is reasonable close to Romanian and French)				

Levels: A1/A2: Basic user - B1/B2: Independent user - C1/C2 Proficient user
Common European Framework of Reference for Languages

Communication

Outstanding verbal and written communications skills in Romanian, English and French, both technically as well as with internal and external stakeholders (management/negotiations).
Highly experienced at giving technical presentations to large audiences (supported by over 370 presentations, out of which over 180 invited keynote/tutorials/lectures).

Organisational/managerial

Proven management experience for over 20 years, with more than10 years in administrative positions

- PI/co-PI on research grants totalling over US$ 51M
- President of Spring Software Consult (1990-1991)
- Chief Technical Officer of RN2R/Rose Research (1998-2001)
- Chair of the Computer Engineering Department, College of IT, UAEU (2005-2006)
- Associate Dean for Research and Graduate Studies, College of IT, UAEU (2006-2011)

Job-related

Teaching experience spanning 23 years (excluding full-time research positions) as follows: 1983-1991 (UPB), 2001-2005 (WSU), 2005-2015 (UAEU), 2015-2016 (UAV)

- Supervised 33 MSc, 1 PhD, and 1 PostDoc
- Evaluator (committee member) for 8 PhDs (Univ. Ulster, Univ. Oslo, Univ. Paris Sud)
- Contributed significantly to 2 successful ABET accreditations (in 2003 while with WSU, and in 2011 while with UAEU)
- Proposed/developed many new courses and several new programs (both at the undergraduate and at the graduate level, including the PhD program at UAEU)

Digital competence

SELF-ASSESSMENT				
Information processing	Communication	Content creation	Safety	Problem solving
Proficient user	Proficient user	Proficient user	Independent user	Independent user

Levels: Basic user - Independent user - Proficient user
Digital competences - Self-assessment grid

Baccalaureate in CS followed by MSc, PhD and two Postdocs in CE

Highly familiar (have used these over many years) with:

- Fortran, Cobol, Prolog
- Assembly languages (ASIRIS, ASM86, MIPS)
- Matlab
- Cadence, Spice, LEdit, VHDL, Simon
- Corel (suite)

Driving licence

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ADDITIONAL INFORMATION

Publications

In reverse chronological order

2 books

– V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures
Book in progress (contract signed with World Scientific)

– V. Beiu: VLSI Complexity of Discrete Neural Networks
Book in progress (contract signed with Taylor & Francis)

– V. Beiu, R. Andonie, and R. Dogaru: Fundamental Problems of Neural Networks
Book in progress (contract signed with Technical Printing House)

B_2 V. Beiu, and S. Harous (Eds.), ISBN 978-1-4799-7212-8
Innovations, IEEE Press, November 2014 1–132

B_1 A. Schmid, S. Goel, W. Wang, V. Beiu, and S. Carrara (Eds.), ISBN 978-3-642-02427-6
Nano-Net, Springer, LNICS, October 2009 1–286

PhD V. Beiu: Neural Networks Using Threshold Gates
A Complexity Analysis of Their Area- and Time-Efficient VLSI Implementations
PhD dissertation, Katholieke Universiteit Leuven, Leuven, Belgium
U.D.C. 621.3.04977: 681.3*C13 (x-27-151779-3), May 1994 1–222

8 chapters **7 Invited** **2 (Ch_1 and Ch_3) are in ISI Web of Science (Thompson Reuters)**

– V. Beiu, and W. Ibrahim: On Enabling Redundant Designs for Nano Computations
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– V. Beiu, J.M. Quintana, and M.J. Avedillo
Threshold Logic Design and Implementations: From the Early Days into the Nanoera
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– M.H. Sulieman, and V. Beiu
From Single Electron Technology (SET) Full Adders to Optimal Practical SET Adders
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– V. Beiu, and U. Rückert: Roadmap for Nano Architectures
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

– J. Nyathi, and V. Beiu: Advanced Techniques for Reducing Power Consumption
In V. Beiu, and U. Rückert (Eds.): Emerging Brain-Inspired Nano-Architectures

Ch_8 V. Beiu, L. Zhang, A. Beg, W. Ibrahim, and M. Tache:
Axon-Inspired Communication Systems **$Invited_7$**
Chapter 15 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications
Handbook, CRC Press / Taylor & Francis Group (UK and USA), June 2013 193–208

Ch_7 A. Beg, M.H. Sulieman, V. Beiu, and W. Ibrahim: Low-Power Reliable Nano Adders **$Invited_6$**
Chapter 6 in J.E. Morris and K. Iniewski (Eds.): Nanoelectronic Device Applications
Handbook, CRC Press / Taylor & Francis Group (UK and USA), June 2013 67–75

Ch_6 V. Beiu, W. Ibrahim, and S. Lazarova-Molnar
On Device-level Majority von Neumann Multiplexing **$Invited_5$**
In J.R. Rabuñal et al. (Eds.): Encyclopedia of Artificial Intelligence
IGI Global, USA (Hershey, PA) and UK (London), 2009, Chapter 72 471–479

Ch_5 V. Beiu, and W. Ibrahim
On Computing Nano-Architectures Using Unreliable Nano-Devices **$Invited_4$**
In S.E. Lyshevski (Ed.): Nano- and Molecular-Electronics Handbook
Taylor and Francis (UK and USA), May 2007, Chapter 12 1–49

Ch_4 V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency **$Invited_3$**
In R. Andonie, and D. Grosu (Eds.): Neural Priorities in Data Transmission and EDA
Tempus SJEP 8180-94, "Transilvania" Univ. of Braşov, Braşov, Romania, 1998 38–74

Ch_3 V. Beiu: Constant Fan-in Discrete Neural Networks Are VLSI-Optimal
In S.W. Ellacott, J.C. Mason, and I.J. Anderson (Eds.)
Mathematics of Neural Networks Models, Algorithms and Applications
Kluwer Academic, Boston, MA, USA, 1997, Chapter 12 89–94

Ch_2 V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks) **$Invited_2$**
In E. Fiesler, and R. Beale (Eds.): Handbook of Neural Computations
Institute of Physics, New York, NY, USA, 1996, Chapter E1.4 E1.4.1–34

Ch_1 V. Beiu: Optimal VLSI Implementations of Neural Networks **$Invited_1$**
In J.G. Taylor (Ed.): Neural Networks and Their Applications
John Wiley & Sons, Chichester, UK, 1996, Chapter 18 255–276

11 patents — **10 (P_2 – P_{11}) are in ISI Web of Science (Thompson Reuters)**

– V. Beiu: Procedure Enabling Statistical Meaningful Evaluation of Any Physical Feature or Figure-of-Merit of a Digital or Analog Circuit
UAEU Intellectual Property (disclosure), July 16, 2014 & February 11, 2015 — Submitted

P_{11} V. Beiu
Low-Power Differential Conductance-Based Logic Gate and Method of Operation Thereof
US 6,580,296, June 17, 2003 — 1–18

P_{10} V. Beiu: Microprocessor and a Digital Signal Processor Including Adder and Multiplier Circuits Employing Logic Gates Having Discrete and Weighted Inputs
US 6,516,331, February 4, 2003 — 1–14

P_9 V. Beiu: Adder Circuits Employing Logic Gates Having Discrete Weighted Inputs and a Method of Operation Therewith
US 6,502,120, December 31, 2002 — 1–13

P_8 V. Beiu
Adder Having Reduced Number of Internal Layers and Method of Operation Thereof
US 6,438,572, August 20, 2002 [Also as WO/2001/023992 and AU40251/01] — 1–11

P_7 V. Beiu: Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and Manufacturing Thereof
US 6,430,585, August 6, 2002 [Also as WO/2001/024367 and AU76009/00] — 1–16

P_6 V. Beiu
Adder Having Reduced Number of Internal Layers and Method of Operation Thereof
TW 493139, July 1, 2002 — 1–15

P_5 V. Beiu: Noise Tolerant Conductance-Based Logic Gate and Methods of Operation and Manufacturing Thereof
TW 483249, April 11, 2002 — 1–13

P_4 V. Beiu: Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs and Methods of Performing Combinatorial Operations Therewith
TW 481774, April 1, 2002 — 1–14

P_3 V. Beiu
Logic Gate Having Reduced Power Dissipation and Method of Operation Thereof
US 6,259,275, July 10, 2001 — 1–19

P_2 V. Beiu: Adder and Multiplier Circuits Employing Logic Gates Having Discrete, Weighted Inputs and Methods of Performing Combinatorial Operations Therewith
US 6,205,458, March 20, 2001 [Also as WO/2000/017802 and AU58155/99] — 1–14

P_1 V. Beiu: LSI Unit for Mutual Exclusion
RO 84763, April 26, 1984 — 1–12

28 journals — **2 Invited** — **17 are in ISI Web of Science (Thompson Reuters)**

– V. Beiu et al.
The Curse of Constant Failure Rates, Inputs and Averaging – A Comprehensive Review
TBD (probably IEEE Transactions on Reliability, IF~1.9, SJR~1.7) — In planning

– V. Beiu et al.: On Schmitt Trigger Range of Applications
TBD (probably IEEE Transactions on VLSI Systems, IF~1.3, SJR~1) — In planning

– V. Beiu
Brain-inspired Computing Revisited – Why modeling is still needed more than ever
TBD (Frontiers in Neuroscience / Proc. IEEE / PNAS, IF~3.7 / 4.9 / 9.7) — In progress

– V. Beiu
Brain-inspired Computing Revisited – Why energy consumption is so elusive
TBD (Frontiers in Neuroscience / Proc. IEEE / PNAS, IF~3.7 / 4.9 / 9.7) — In progress

– V. Beiu: The Trustworthy Wings of the Mysterious Butterflies
TBD (probably Nature, IF~40, SJR~17) — In progress

– S.R. Cowell, V. Beiu, L. Dauş, and P. Poulin
On Exact Reliability Enhancements of Small Hammock Networks
IEEE Transactions on Reliability (IF~1.9, SJR~1.7) — Submitted

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Best Paper Award$_5$ 721–725

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O_{36} R.M. Beiu, C.D. Stanescu, and V. Beiu
Nanostructured Fiber Optics as Highly Sensitive Mechanical Sensors
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007
Invited$_7$

O_{35} W. Ibrahim, and V. Beiu: A Hybrid Monte-Carlo and Numerical Simulations Approach for Future Nano-circuits Reliability Calculation
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O_{34} S. Lazarova-Molnar, V. Beiu, and W. Ibrahim
Proxels for Reliability Assessment of Future Nano-Circuits
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O_{33} H. Amer, and V. Beiu
On Global Communications for Nano-Architectures – Brain versus Rent's Rule
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O_{32} B.A.M. Madappuram, and V. Beiu
Using Standing Waves for Communications Might Work for Crossbar Architectures
International Trends in NanoTechnology Conference TNT'07
San Sebastian, Spain, September 3-7, 2007

O_{31} M.H. Sulieman, and V. Beiu
Investigating the Reliability of Single-Electron-Technology Gates and Circuits
UAEU Annual Research Conference ARC-8, Al Ain, UAE, April 23-25, 2007

O_{30} J. Nyathi, V. Beiu, and S. Aunet
Sub Femto Joule Switching – High Speed Reliable CMOS Circuits Are Feasible
ASILOMAR Conference on Signal, Systems and Computers
Pacific Groove, CA, USA, November 7-10, 2004

O_{29} J. Nyathi, V. Beiu, and S. Aunet
Femto Joule Switching – Review of Low Energy Design Styles for the Nano Era **Invited$_6$**
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM'04
Krakow, Poland, September 13-17, 2004

O_{28} V. Beiu, U. Rückert, S. Roy, and J. Nyathi
On Nanoelectronic Architectural Challenges and Plausible Solutions
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM'04
Krakow, Poland, September 13-17, 2004

O_{27} V. Beiu, and A. Zawadzki
Why VLSI/Nano Library Design Should Use Kolmogorov's Superpositions
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM'04
Krakow, Poland, September 13-17, 2004

O_{26} V. Beiu: On Biological and Hardware Neural Networks **Invited$_5$**
International Joint Meeting AMS-SMM, Denton, TX, USA, May 19-22, 1999

O_{25} V. Beiu, J. Frigo, and K.R. Moore: Why the Nervous Networks Are Reliable
International Symposium on Artificial Intelligence and Adaptive Systems CIMAF'99
Havana, Cuba, March 24-28, 1999

O_{24} V. Beiu, J. Frigo, and K.R. Moore: On the Reliability of Nervous Nets
International Conference on Computational Intelligence for Modeling,
Control and Automation CIMCA'99, Vienna, Austria, February 17-19, 1999

O_{23} S. Draghici, and V. Beiu: On Issues Related to VLSI Implementations of Neural Networks
International Conference on Cognitive and Neural Systems CNS'98
Boston, MA, USA, May 27-30, 1998

O_{22} D.O. Creteanu, and V. Beiu: Systolic Pattern Recognition System
International Conference on Fuzzy Systems and Artificial Intelligence IFSAI'92
Iaşi, Romania, October 28-31, 1992

O_{21} V. Beiu, D.C. Ioan, M. Dumbrava, and O. Robciuc
Physical Fields Determination Using Continuous Boltzmann Machines **Invited$_4$**
Symposium on Parallel Computing, Bucharest, Romania, December 10-11, 1991

O_{20} V. Beiu: Motion Detection with Neural Networks
International Conference on Industrial and Applied Mathematics ICIAM'91
Washington DC, USA, July 8-12, 1991

O_{19} V. Beiu: Neural Network Solutions for Motion Detection
International Symposium on Applied Informatics, Innsbruck, Austria, February 18-21, 1991

O_{18} A. Florea, V. Beiu, and S. Georgescu
Expert System Development with a Neural Network Simulator
International Conference on AI and Control Systems for Robots AICSR'89
Strbskoe Pleso, Czechoslovakia, November 6-10, 1989

O_{17} V. Beiu: From Systolic Arrays to Neural Networks **Invited$_3$**
International Symposium on Informatics INFO-IASI'89
Iaşi, Romania, October 19-21, 1989

O_{16} M. Constantinescu, and V. Beiu
Theoretical Aspects of Parallel Algorithms for Histogram Modification
International Conference on Computer Systems MICROSYSTEM'89
Carlsbad (Karlovy Vary), Czechoslovakia, September 18-21, 1989

O_{15} V. Beiu, and S. Georgescu: Neural Network Models of Vision
IAPR Workshop on Computer Vision, Tokyo, Japan, October 12-14, 1988

O_{14} A. Florea, and V. Beiu: Expert Decisions Using Neural Models
Conference on Electronics, Telecommunication, Control and Computers CNETAC'88
Bucharest, Romania, December 7-9, 1988

O_{13} V. Beiu: Hierarchical Memory Enhanced with List Processing Facilities
International Conference on Computer Systems MICROSYSTEM'88
Bratislava, Czechoslovakia, August 30 - September 1, 1988

O_{12} V. Beiu: Parallel Line-Drawing Algorithms
International Conference on Computer Systems MICROSYSTEM'88
Bratislava, Czechoslovakia, August 30 - September 1, 1988

O_{11} V. Beiu. M. Ionescu, E. Paşol, and L. Zuzu
VLSI Implementation of a Statistical Multiplexer
International Symposium Mini and Microcomputers ISMM-MIMI'87
Lugano, Switzerland, June 29 - July 2, 1987

O_{10} V. Beiu, M. Ionescu, E. Paşol, and L. Zuzu
Adaptive Multiplexing Algorithm and Its Possible VLSI Implementation
Mediterranean Electrotechnical Conference MELECON'87, Rome, Italy, March 24-26, 1987

O_9 V. Beiu: Smart Image Memory for Parallel Line Generation
Conference on Electronics, Telecommunication, Control and Computers CNETAC'86
Bucharest, Romania, December 4-6, 1986

O_8 F. Moraru, C. Ispas, S. Constantin, A. Niculescu, and V. Beiu
Automat Conical Ball Bearing Sorting System
National Conference on Automatic Measurement Systems Using Computer Techniques
Bucharest, Romania, May 22-24, 1986

O_7 V. Beiu: Parallel Adder with Regular Structure
Conference on Electronics, Telecommunication, Control and Computers CNETAC'85
Bucharest, Romania, November 21-23, 1985

O_6 V. Beiu: Self-Testable and Self-Repairable Units – A Must for VLSI Structures
Conference on Electronics, Telecommunication, Control and Computers CNETAC'84
Bucharest, Romania, November 22-24, 1984

O_5 V. Beiu: High Reliability Memory Organization
Conference on Electronics, Telecommunication, Control and Computers CNETAC'83
Bucharest, Romania, November 17-18, 1983

O_4 V. Beiu: Using Microprocessors in Audio Systems
Conference on Electronics, Telecommunication, Control and Computers CNETAC'82
Bucharest, Romania, November 17-19, 1982

O_3 V. Beiu: Memory Structure with Simultaneous Read and Write Capabilities **Invited$_2$**
Military Academy of Sciences, Bucharest, Romania, November, 1982

O_2 V. Beiu: Method for Storing Digital Information on a Video Recorder
Conference on Electronics, Telecommunication, Control and Computers CNETAC'81
Bucharest, Romania, November, 1981

O_1 V. Beiu
Reliability Enhanced Memory Architecture with Gracefully Degrading Performances **Invited$_1$**
Jubilee: Ten Years from the Foundation of the National College of Informatics
Bucharest, Romania, May, 1981

67 technical reports 25 have appeared only as technical reports, while 42 have been published as conferences/journals
Los Alamos Unrestricted Reports are available at http://www.osti.gov/scitech/search/semantic:Beiu/

TR_{67} V. Beiu: WTEC-NANO2 (21 pages)
International Study of the Long-term Impacts and Future Opportunities for
Nanoscale Science and Engineering, September 2010

TR_{66} V. Beiu, H.E. Makaruk, D. Morgan, and L. Popa-Simil
ARGOS Advanced RTR (Real Time Radiography) Graphical Object Selection
Los Alamos Unrestricted Report LA-UR-03-2477, April 2003

TR_{65} V. Beiu, H.E. Makaruk, D. Morgan, and L. Popa-Simil: ARGOS – The Problem
Los Alamos Unrestricted Report LA-UR-03-2474, April 2003

TR_{64} V. Beiu: On Automatic Synthesis of Analog/Digital Circuits
Los Alamos Unrestricted Report LA-UR-98-3463, 1998

TR_{63} V. Beiu: Larger Bases and Mixed Analog/Digital Neural Networks
Los Alamos Unrestricted Report LA-UR-98-3462, 1998

TR_{62} V. Beiu, J. Frigo, and K.R. Moore: On the Reliability of Nervous Nets
Los Alamos Unrestricted Report LA-UR-98-3461, 1998

TR_{61} V. Beiu: Neural Inspired Parallel Computations Require Analog Processors
Los Alamos Unrestricted Report LA-UR-98-3325, 1998

TR_{60} V. Beiu, and S. Draghici
Designing Constructive Neural Learning Algorithms Based on Information Entropy Bounds
Los Alamos Unrestricted Report LA-UR-98-3168, 1998

TR_{59} V. Beiu: On Kolmogorov's Superposition and Boolean Functions
Los Alamos Unrestricted Report LA-UR-98-2883, 1998

TR_{58} V. Beiu: 2D Neural Hardware vs 3D Biological Ones
Los Alamos Unrestricted Report LA-UR-98-2504, 1998

TR_{57} V. Beiu, S. Draghici, and T. De Pauw: A Constructive Approach to Calculating Lower Entropy Bounds
Los Alamos Unrestricted Report LA-UR-98-2333, 1998

TR_{56} V. Beiu: Implementing Size-Optimal Discrete Neural Networks Requires Analog Circuitry
Los Alamos Unrestricted Report LA-UR-98-1702, 1998

TR_{55} V. Beiu, and K.R. Moore: On Analog Implementation of Discrete Neural Networks
Los Alamos Unrestricted Report LA-UR-98-1609, 1998

TR_{54} V. Beiu: How to Build VLSI-Efficient Neural Chips
Los Alamos Unrestricted Report LA-UR-97-4460, 1997

TR_{53} V. Beiu: Implementing Size-Optimal Discrete Neural Networks Requires Analog Circuitry
Los Alamos Unrestricted Report LA-UR-97-4432, 1997

TR_{52} V. Beiu, and H.E. Makaruk: On Deeper Nets for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-4413, 1997

TR_{51} V. Beiu, and H.E. Makaruk: Deeper and Sparser Nets Are Optimal
Los Alamos Unrestricted Report LA-UR-97-4359, 1997

TR_{50} V. Beiu, S. Draghici, and H.E. Makaruk: On Limited Fan-In Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-4314, 1997

TR_{49} V. Beiu, and H.E. Makaruk
Constructive Entropy Bounds Based on n-Dimensional Complexes
Los Alamos Unrestricted Report LA-UR-97-4251, 1997

TR_{48} V. Beiu, and H.E. Makaruk: Small Fan-In Is Beautiful
Los Alamos Unrestricted Report LA-UR-97-3493, 1997

TR_{47} V. Beiu: On the Circuit and VLSI Complexity of Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-97-3353, 1997

TR_{46} V. Beiu, and S. Draghici: On Sparsely Connected Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-2970, 1997

TR_{45} V. Beiu, and H.E. Makaruk: Computing Volumes of n-Dimensional Complexes
Los Alamos Unrestricted Report LA-UR-97-2873, 1997

TR_{44} V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency
Los Alamos Unrestricted Report LA-UR-97-2843, 1997

TR_{43} V. Beiu: The Next Generation of Neural Networks Chips
Los Alamos Unrestricted Report LA-UR-97-1917, 1997

TR_{42} V. Beiu: When Reduced Connectivity Neural Networks Are Complexity Optimal?
Los Alamos Unrestricted Report LA-UR-97-1916, 1997

TR_{41} V. Beiu: Digital Integrated Circuit Implementations (of Neural Networks)
Los Alamos Unrestricted Report LA-UR-97-1900, 1997

TR_{40} V. Beiu: Enhanced Lower Entropy Bounds with Application to Constructive Learning
Los Alamos Unrestricted Report LA-UR-97-1877, 1997

TR_{39} S. Draghici, V. Beiu, and I.K. Sethi: A VLSI Optimal Constructive Algorithm for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-1609, 1997

TR_{38} V. Beiu, and S. Draghici: On Sparsely Connected Optimal Neural Networks
Los Alamos Unrestricted Report LA-UR-97-1567, 1997

TR_{37} V. Beiu: When Constants Are Important
Los Alamos Unrestricted Report LA-UR-97-1262, 1997

TR_{36} V. Beiu, S. Draghici, and T. De Pauw: A Constructive Approach to Calculating Lower Entropy Bounds
Los Alamos Unrestricted Report LA-UR-97-884, 1997

TR_{35} V. Beiu: Optimization of Circuits Using a Constructive Neural Network Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-851, 1997

TR_{34} V. Beiu: Enhanced Lower Entropy Bounds with Application to Constructive Learning
Los Alamos Unrestricted Report LA-UR-97-516, 1997

TR_{33} V. Beiu: Reduced Complexity Constructive Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-515, 1997

TR_{32} S. Draghici, and V. Beiu: Entropy Based Comparison of Neural Networks for Classification
Los Alamos Unrestricted Report LA-UR-97-483, 1997

TR_{31} V. Beiu, and S. Draghici: Limited Weights Neural Networks: Very Tight Entropy Based Bounds
Los Alamos Unrestricted Report LA-UR-97-294, 1997

TR_{30} V. Beiu: When Constants Are Important
Los Alamos Unrestricted Report LA-UR-97-226, 1997

TR_{29} V. Beiu: Constant Fan-In Discrete Neural Networks Are VLSI-Optimal
Los Alamos Unrestricted Report LA-UR-97-61, 1997

TR_{28} V. Beiu, and T. De Pauw: Tight Bounds on the Size of Neural Networks for Classification Problems
Los Alamos Unrestricted Report LA-UR-97-60, 1997

TR_{27} V. Beiu: Optimization of Circuits Using a Constructive Neural Network Learning Algorithm
Los Alamos Unrestricted Report LA-UR-97-59, 1997

TR_{26} V. Beiu: On the Circuit and VLSI Complexity of Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-96-3591, 1996

TR_{25} V. Beiu: New VLSI Complexity Results for Threshold Gate COMPARISON
Los Alamos Unrestricted Report LA-UR-96-3576, 1996

TR_{24} J.C. Lemm, V. Beiu, and J.G. Taylor
Density Estimation as a Preprocessing Step for Constructive Algorithms
Munster University Technical Report MS-TPI-95-10, 1995

TR_{23} V. Beiu, D.C. Ioan, M. Dumbrava, and O. Robciuc
Physical Fields Determination Using Continuous Boltzmann Machines
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1991

TR_{22} V. Beiu: Motion Detection with Neural Networks
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, September 1991

TR_{21} V. Beiu: Neural Network Solutions for Motion Detection
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, March 1991

TR_{20} V. Beiu: Neural Network Priority Queue
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, October 1990

TR_{19} A. Florea, V. Beiu, and S. Georgescu: Expert System Development with a Neural Network Simulator
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1989

TR_{18} V. Beiu: From Systolic Arrays to Neural Networks
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, November 1989

TR_{17} M. Constantinescu, and V. Beiu: Theoretical Aspects of Parallel Algorithms for Histogram Modification
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, October 1989

TR_{16} V. Beiu, and A. Florea: Basic Structure of a Program Used to Simulate Processor Networks
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1988

TR_{15} A. Florea, and V. Beiu: Expert Decisions Using Neural Models
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1988

TR_{14} V. Beiu: Hierarchical Memory Enhanced with List Processing Facilities
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, October 1988

TR_{13} V. Beiu: Parallel Line-Drawing Algorithms
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, October 1988

TR_{12} V. Ivanov, and V. Beiu: Heuristic Simulation of Circuits Using PROLOG
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, February 1988

TR_{11} V. Beiu, M. Ionescu, E. Paşol, and L. Zuzu: VLSI Implementation of a Statistical Multiplexer
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, September 1987

TR_{10} V. Beiu, M. Ionescu, E. Paşol, and L. Zuzu
Adaptive Multiplexing Algorithm and Its Possible VLSI Implementation
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, April 1987

TR_{9} V. Beiu: Smart Image Memory for Parallel Line Generation
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1986

TR_{8} F. Moraru, C. Ispas, S. Constantin, A. Niculescu, and V. Beiu: Automat Conical Ball Bearing Sorting System
Technical Report, Department of Mechanics, University “Politehnica” of Bucharest, Romania, June 1986

TR_{7} V. Beiu: Parallel Adder with Regular Structure
Technical Report, CSE Department, University “Politehnica” of Bucharest, Romania, December 1985

TR_6 V. Beiu: Self-Testable and Self-Repairable Units: A Must for VLSI Structures
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1984

TR_5 V. Beiu: Highly Reliable Memory Organization
Technical Report, CSE Department, University "Politehnica" of Bucharest, Romania, December 1983

TR_4 V. Beiu: Memory Structure with Simultaneous Read and Write Capabilities
Technical Report, Military Academy of Sciences, Bucharest, Romania, November 1982

TR_3 V. Beiu: Using Microprocessors in Audio Systems
Technical Report, Research Institute for Computer Technique, Bucharest, Romania, December 1982

TR_2 V. Beiu: Method for Recording Digital Information on a Video Recorder
Technical Report, Research Institute for Computer Technique, Bucharest, Romania, December 1981

TR_1 V. Beiu: Reliability Enhanced Memory with Gracefully Degrading Performances
Technical Report, Research Institute for Computer Technique, Bucharest, Romania, July 1981

Invited presentations

17 invited keynotes/plenaries

– V. Beiu: Brain versus Computer Revisited — Keynote
Asia-Pacific Conference on Electrical Electronics and Engineering AEEE'16
Postponed to 2016 [invitation to AEEE'15, Dubai, UAE, November 18-19, 2015]

K_{17} V. Beiu: Why the Brain Can and the Computer Can't — Keynote
IEEE International Workshop on Soft Computing Applications SOFA'16
Arad, Romania, August 24-26, 2016, http://sofa2016.org/prog.html

K_{16} V. Beiu — Keynote
On the Reliability Accuracy Challenge − Grappling with a Seemingly Intractable Problem
European Dependable Computing Conference EDCC'12
Sibiu, Romania, May 8-11, 2012

K_{15} T.G. Noll, P. Horn, N. Menezes, V. Beiu, and D. Hammerstrom — Panel
Alternative Minimum-Energy Computing Paradigms (Brain-inspired Information Processors)
International Forum on Minimum Energy Electronic Systems MEES'10
Abu Dhabi, UAE, May 23-24, 2010, http://www.src.org/calendar/e003960/ [Session V]

K_{14} V. Beiu — Keynote
Trustworthy Wings of the Mysterious Butterflies (Brain-inspired Information Processing)
International Nanotechnology Conference on Communication and Cooperation INC6
Grenoble, France, May 19, 2010
http://www.minatec.org/inc6/presentations/We1-1_Beiu.pdf

K_{13} V. Beiu — Keynote
Connectivity and Scalability Issues for Biologically Plausible Nano-electronic Systems
International Workshop on Brain-Inspired Electronic Circuits and Systems BIECS'09
European Solid-State Device Research Conference ESSDERC'09
Athens, Greece, September 18, 2009

K_{12} C. Constantinescu, J.A. Abraham, V. Beiu, H. Naeimi, A. Somani, and S. Wang — Panel
Scaling Towards Nanometer Size Devices – Issues and Solutions
Workshop on Dependable and Secure Nanocomputing WDSN'09 (IEEE / IFIP DSN'09)
Estoril/Lisbon, Portugal, June 29, 2009
http://webhost.laas.fr/TSF/WDSN09/WDSN09_files/Slides/WDSN09_12-Beiu.pdf

K_{11} V. Beiu: Electrons Behaving Badly — Plenary
Information Electronics Systems Global Center of Excellence GCoE'08
Tohoku University, Sendai, Japan, July 14, 2008

K_{10} S. Bhabhu, R.A. Parekhji, M. Nicolaidis, V. Beiu, and M.Y. Zhang — Panel
Mitigating Reliability, Yield and Power Issues in Nano-CMOS: Design or EDA Problem?
IEEE International VLSI Test Symposium VTS'08, San Diego, CA, USA, April 30, 2008

K_9 V. Beiu: Quo Vadis Nano-electronics — Plenary
Information Electronics Systems Global Center of Excellence GCoE'07
Tohoku University, Sendai, Japan, November 27, 2007

K_8 V. Beiu: What Do Shannon, von Neumann, Kolmogorov, and Feynman
Have to Do with ... Moore? — Plenary
IEEE International Symposium on Multiple Valued Logic ISMVL'07
Oslo, Norway, May 14, 2007

K_7 V. Beiu: What Do Moore, von Neumann and Kolmogorov Have in Common? — Keynote
IEEE International Conference on Computer Systems and Applications AICCSA'06
Sharjah, UAE, March 9, 2006

K_6 V. Beiu: The Quest for Reliable Nano Computations — Plenary
IEEE International Conference on Microelectronics ICM'05
Islamabad, Pakistan, December 13, 2005

K_5 U. Rükert, and V. Beiu: Neural Inspired Architectures for Nanoelectronics — Plenary
IEEE International Conference on Intelligent Computing and Information Systems ICICIS'05
Cairo, Egypt, March 5-7, 2005

K_4 V. Beiu: On Biological and Hardware Neural Networks — Keynote
International Joint Meeting of the AMS and SMM, Denton, TX, USA, May 21, 1999

K_3 V. Beiu: 2D Neural Hardware vs 3D Biological Ones — Plenary
International ICSC Symposium on Neural Computations NC'98
Vienna, Austria, September 22, 1998

K_2 V. Beiu: Neural Inspired Parallel Computations Require Analog Processors — Plenary
International Conference on Parallel Computing and Electrical Engineering PARELEC'98
Bialystok, Poland, September 4, 1998

K_1 V. Beiu: How to Build VLSI-Efficient Neural Chips — Keynote
International ICSC Symposium on Engineering of Intelligent Systems EIS'98
Tenerife, Canary Islands, Spain, February 9-13, 1998

17 invited tutorials

T_{17} V. Beiu, S.R. Cowell, L. Dauş, and P. Poulin: The Brain and the Computer Revisited Once Again
IEEE International Nanotechnology Conference IEEE-NANO'16
Sendai, Japan, August 22, 2016

T_{16} V. Beiu, P.M. Kelly, and W. Ibrahim: On Brain Inspired Nano Interconnects
IEEE International Joint Conference on Neural Networks IJCNN'10 (part of WCCI'10)
Barcelona, Spain, July 18, 2010
http://cis.ieee.org/cis-educational-repository/cis-video-collection/cis-video-library.html?vid=35056547
http://cis.ieee.org/cis-educational-repository/cis-video-collection/cis-video-library.html?vid=35056562

T_{15} V. Beiu, and P.M. Kelly: On Brain Inspired Interconnects for Nano-electronics
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 19, 2009

T_{14} V. Beiu, and W. Ibrahim: On Reliability When Down to a Handful of Electrons
IEEE International Nanotechnology Conference IEEE-NANO'09
Genoa, Italy, June 27, 2009

T_{13} V. Beiu: On Brain Inspired Low-Power Redundant Designs for Silicon Nano-electronics and Beyond
IEEE Annual Conference of the Industrial Electronic Society IECON'07
Taipei, Taiwan, November 5, 2007

T_{12} V. Beiu: On Brain-Inspired Redundant Designs
IEEE International Conference on Design and Technology of Integrated Systems DTIS'07
Rabat, Morocco, September 2, 2007

T_{11} V. Beiu, and W. Ibrahim:
Dealing with the Reliability Challenge for Semiconductor Nano-electronics and Beyond
IEEE International Midwest Symposium on Circuits and Systems MWSCAS'07
Montreal, Canada, August 5, 2007

T_{10} V. Beiu, and W. Ibrahim: Emerging Fault-Tolerant Designs for Novel Nano-Architectures
IEEE International Conference on Nanotechnology IEEE-NANO'07
Hong Kong, China, August 2, 2007

T_9 V. Beiu, J. Nyathi, S. Aunet, and M.H. Sulieman: Femto Joule Switching for Nano Electronics
IEEE International Conference on Computer Systems and Applications AICCSA'06
Sharjah, UAE, March 8-11, 2006

T_8 V. Beiu: Design Challenges for Nanoelectronics
International Conference on Innovations in Information Technologies IIT'05
Dubai, UAE, September 26-28, 2005

T_7 V. Beiu, and S. Roy: Practical Redundant Designs for Nano Architectures – Novel Theoretical Results
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM'04
Krakow, Poland, September 17, 2004

T_6 V. Beiu, J.M. Quintana, M.J. Avedillo, and P.-S. Wu
Threshold Logic From Vacuum Tubes to Nanoelectronics
IEEE International Conference on Neural Networks and Signal Processing ICNNSP'03
Nanjing, China, December 14-17, 2003

T_5 V. Beiu, J.M. Quintana, and M.J. Avedillo: Threshold Logic – From TTL to Quantum Computing
IEEE International Joint Conference on Neural Networks IJCNN'03
Portland, OR, USA, July 20-24, 2003

T_4 V. Beiu: How to Build VLSI-Efficient Neural Chips
International ICSC Symposium on Engineering of Intelligent Systems EIS'98
Tenerife, Canary Islands, Spain, February 9-13, 1998

T_3 V. Beiu: Kolmogorov's Superpositions and New Mixed Analog/Digital Architectures
Brazilian Symposium on Neural Networks IV SBRN, Goiania, Brazil, December 4, 1997

T_2 V. Beiu: Entropy, Constructive Neural Learning, and VLSI Efficiency
International Workshop on Neural Research Priorities in Data Transmission and EDA NEuroTop'97
Braşov, Romania, May 27, 1997

T_1 V. Beiu: Overview of the Present State-of-the-Art of Hardware Implementations of Neural Networks
Brazilian Symposium on Neural Networks SBRN'96, Recife, Brazil, November 13, 1996

44 invited lectures/seminars

L_{44} V. Beiu: What's All the Fuss About the Brain?
CIT Graduate Seminar, UAEU, Al Ain, UAE, May 27, 2015

L_{43} V. Beiu: Revealing the Reliability Scheme of the Neurons – One Ion Channel at a Time
UAEU Cognitive Science Research Series, UAEU, Al Ain, UAE, May 24, 2015

L_{42} V. Beiu: If Biology Can … Why Can't Silicon? The Brain and the Computer
TU Dresden, Dresden, Germany, July 11, 2013
http://nano.tu-dresden.de/pages/seminar_637.html

L_{41} V. Beiu: The Brain – A Gentle Introduction Clearing Misconceptions
TU Dresden, Dresden, Germany, April 11, 2013
http://nano.tu-dresden.de/pages/seminar_623.html

L_{40} V. Beiu: From Ion Channels to Future Nano-Architectures −
Beyond von Neumann Cellular Automata
Chalmers University, Gothenburg, Sweden, November 2, 2012

L_{39} V. Beiu: Bio-inspired Arrays to the Rescue −
The Curse of Constant Failure Rates and Gaussian Distributions
Chalmers University, Gothenburg, Sweden, October 29, 2012
http://www.chalmers.se/mc2/symone-en/events/kickoff-workshop-30-31

L_{38} V. Beiu: On the Reliability Accuracy Challenge
University of Ulster, Magee, UK, December 16, 2011

L_{37} V. Beiu: Reliability Prospects for Ultra Low Power Hybrid NEMS-CMOS
UC Berkeley, Berkeley, CA, November 14, 2011

L_{36} V. Beiu: On Biologically Inspired Processing = Communication + Computation
University of Ulster, Magee, UK, November 19, 2010

$L_{34\text{-}35}$ V. Beiu: Brain Inspired Nano Architectures — Electron Behaving Badly
– IEEE P/T Colloquium, Los Alamos National Laboratory, Los Alamos, NM, USA, April 15, 2008
– CIT Distinguished Lecture Series, College of IT, UAEU, Al Ain, UAE, March 13, 2008

L_{33} V. Beiu: On Brain Inspired Low-Power Redundant Designs for Silicon Nano-electronics and Beyond
Khalifa University of Science, Technology and Research (KUSTAR), Sharjah, UAE, March 3, 2008

L_{32} V. Beiu: Fault Tolerant Brain Inspired Nano Architectures
CIT Distinguished Lecture Series, College of IT, UAEU, Al Ain, UAE, April 2006

L_{31} V. Beiu: On Brain Inspired Nano Architectures — There Are Plenty of Opportunities at the Top
University of Ulster, Londonderry, UK, November 25, 2005

L_{30} V. Beiu: Great Challenges of Nanoelectronics — There Are Plenty of Challenges at the Bottom
University of Ulster, Londonderry, UK, November 23, 2005

L_{29} V. Beiu: Achieving High-Speeds at Ultra Low-Power – Femto Joule Switching Nano Architectures
Heinz Nixdorf Institute/University of Paderborn, Paderborn, Germany, August 16, 2004

L_{28} V. Beiu: Highly Reliable Designs for Scaled CMOS and Other Nanodevices (SETs, RTDs, Molecular)
Heinz Nixdorf Institute/University of Paderborn, Paderborn, Germany, August 13, 2004

L_{27} V. Beiu: Review of Nanoelectronic Challenges and Some Plausible Solutions
University "Politehnica" of Bucharest, Bucharest, Romania, August 9, 2004

L_{26} V. Beiu: On Novel (neural-inspired) Nano Architectures
Washington State University, Pullman, WA, USA, November 7, 2003

$L_{24\text{-}25}$ V. Beiu: Threshold Gates From TTL to Quantum Computing (Part I and Part II)
– Heinz Nixdorf Institute/University of Paderborn, Paderborn, Germany, July 2, 2003
– University of Paderborn, Paderborn, Germany, July 3, 2003

L_{23} V. Beiu: Advanced Real-Time-Radiography Graphical Object Selection (ARGOS)
Washington State University, Pullman, WA, WA, USA, November 6, 2002

L_{22} V. Beiu: On VLSI Neural Computations
Washington State University, Pullman, WA, USA, October 22, 2001

L_{21} V. Beiu: FastLogic and Its Applications
Berkeley Wireless Research Center (BWRC), Berkeley, CA, USA, November 13, 2001

L_{20} V. Beiu: Neural Gates – Noise Robust but Fan-in Limited
University "Politehnica" of Bucharest, Bucharest, Romania, June 4, 2001

L_{19} V. Beiu: Neural Inspired Parallel Computations Require Analog Processors
Centre National de la Recherche Scientifique (CNRS), Paris, France, September 18, 1998

L_{18} V. Beiu: Introduction to Hardware Implementations of Neural Networks (series of 3 lectures)
State University of Sao Paulo, Sao Paulo, Brazil, December 8-10, 1997

$L_{15\text{-}17}$ V. Beiu: Kolmogorov's Superpositions, Computer Architectures, and VLSI CAD
– Dalle Molle Institute for Perceptual AI (IDIAP), Martigny, Switzerland, October 2, 1997
– Paderborn University, Paderborn, Germany, September 30, 1997
– Heinz Nixdorf Institute (HNI), Paderborn, Germany, September 29, 1997

L_{14} V. Beiu: 2D Neural Network Hardware vs 3D Biological Ones
University Paris XII, Paris, France, September 22, 1997

L_{13} V. Beiu: Optimal Synthesis of Neural Circuits Using a Construction for Kolmogorov's Superpositions
King's College London, London, UK, June 13, 1997

L_{12} V. Beiu: On Constructing Size- and VLSI-Optimal Neural Networks
Royal Holloway University, Egham, UK, June 11, 1997

L_{11} V. Beiu: On Entropy Bounds with Application to Designing Constructive Neural Learning Algorithms
Oxford University, Oxford, UK, June 9, 1997

L_{10} V. Beiu: Entropy and Efficient Neural Learning
University "Politehnica" of Bucharest, Bucharest, Romania, June 2, 1997

L_{9} V. Beiu: Hardware Implementation of Neural Networks – A Comprehensive Review
Los Alamos National Laboratory, Los Alamos, NM, USA, February 7, 1997

L_{8} V. Beiu: Hardware Implementations of Neural Networks – Where Are We, and Where Are We Going?
Series of lectures, University of Pernambuco, Recife, Brazil, November 15-20, 1996

$L_{6\text{-}7}$ V. Beiu: On the Complexity of Area- and Time-Efficient VLSI Implementations of Neural Networks
– Royal Holloway University, Egham, UK, June 12, 1996
– "Transilvania" University of Braşov, Braşov, Romania, December 19, 1995

L_{5} V. Beiu: VLSI-Efficient (Neural) Learning
University "Politehnica" of Bucharest, Bucharest, Romania, May 22, 1995

L_{4} V. Beiu: Hardware Implementations of Neural Networks
Center for Neural Networks, King's College London, London, UK, February 9, 1995

L_{3} V. Beiu: On Efficient Neural VLSI Implementations
University "Politehnica" of Timişoara, Timişoara, Romania, November 21, 1994

L_{2} V. Beiu, and A. Florea: CAD Tools for PCs (series of lectures)
AVERSA SA, Bucharest, Romania, May-June, 1991

L_{1} V. Beiu, and A. Florea: IBM PC Training (series of lectures)
Ministry of National Defense, Bucharest, Romania, March - April, 1991

67 invited presentations (to conferences/universities/labs)

P_{67} V. Beiu: Elucidating the Low Power of the Brain – Why Ions Really Matter
CMOS Emerging Technologies Research CMOSETR'16, Montreal, Canada, May 25-27, 2016
http://www.etcmos.com/files/Conference_Program_2016.pdf

P_{66} V. Beiu, and L. Dauş: Deciphering the Reliability Scheme of the Neurons – One Ion Channel at a Time
International Conference on Bio-inspired Information & Communication Technology BICT'14
Boston, MA, USA, December 1-3, 2014

P_{65} V. Beiu: Bio-Inspired Designing with Arrays – When Distributions are Non-Gaussian
CMOS Emerging Technologies Research CMOSETR'14, Grenoble, France, July 6-8, 2014
http://www.cmosetr.com/past_conferences.php?event=2014 (go to Bioelectronics)
http://books.google.ca/books?id=OL3aAwAAQBAJ&pg=PA102

P_{64} V. Beiu: What's All the Fuss About the Brain? A Few Large Brain Research Projects
Cognitive Society Day, UAEU, Al Ain, UAE, May 20, 2014

P_{63} V. Beiu, A. Beg, and W. Ibrahim: Atto-Joule Gates for the Whole Voltage Range
IEEE International Conference on Nanotechnology IEEE-NANO'11
Portland, OR, USA, August 15-19, 2011

P_{62} V. Beiu: Quo Vadis Nano Architectures [Why U×I Can Be Zero]
The 3rd UAEU Physics Symposium
Al Ain, Abu Dhabi, UAE, May 5, 2011

P_{61} V. Beiu: Ultra Low Power Processing Should Be … Biologically Inspired
Masdar Institute of Science and Technology
Abu Dhabi, UAE, January 10, 2011

P_{60} P.M. Kelly, F. Tuffy, V. Beiu, and L.J. McDaid: Reduced Interconnects in Neural Networks Using a Time Multiplexed Architecture based on Quantum Devices
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 18-20, 2009

P_{59} W. Ibrahim, and V. Beiu: A Bayesian-based EDA Tool for Nano-Circuits Reliability Calculations
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 18-20, 2009

P_{58} V. Beiu, B.A.M. Madappuram, P.M. Kelly, and L.J. McDaid
On Two-layer Hierarchical Networks: How Does the Brain Do This?
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 18-20, 2009

P_{57} V. Beiu, W. Ibrahim, and R.Z. Makki: On Wires Holding a Handful of Electrons
International ICST Conference on Nano-Networks Nano-Net'09
Luzern, Switzerland, October 18-20, 2009

P_{56} V. Beiu, H. Amer, and M. McGinnity
On Global Communications for Nano-Architectures: Brain versus Rent's Rule
IEEE International Conference on Design of Circuits and Integrated Systems DCIS'07
Seville, Spain, November 21-23, 2007

P_{55} R.M. Beiu, C.D. Stanescu, and V. Beiu
Nanostructured Fiber Optics as Highly Sensitive Mechanical Sensors
International Trends in NanoTechnology TNT'07, San Sebastian, Spain, September 3-7, 2007

P_{54} V. Beiu: On Brain-inspired Nano-architectures (Computations and Communications)
An Inescapable Device-level Convergence?
Center on Functional Engineered Nano Architectonics (FENA)
University of California at Los Angeles (UCLA), Los Angeles, CA, USA, April 27, 2007

P_{53} V. Beiu: A Brain-inspired Perspective on Nano-Communications
NanoMaterials'07, San Diego, CA, USA, April 23-25, 2007

P_{52} V. Beiu: The Quest for Redundant Computations –
When Neural-inspired Will Outperform Classical Architectures
NSF Workshop on Architectures for Silicon Nanoelectronics and Beyond
Portland State University, Portland, OR, USA, September 13-14, 2005

P_{51} V. Beiu: From Perceptrons to Neural Inspired Circuits and Nano Architectures
Advanced Research and Development Agency (ARDA)
Oak Ridge National Lab, Knoxville, TN, USA, April 11-12, 2005

$P_{47\text{-}50}$ V. Beiu: From Neural Inspired Gates and Circuits to Nano Architectures
– Centre National de la Recherche Scientifique (CNRS), Paris, France, July 2005
– University of Rochester, Rochester, NY, USA, March 15, 2005
– Rochester Institute of Technology, Rochester, NY, USA, March 14, 2005
– Technical University of Graz, Graz, Austria, March 3, 2005

P_{46} V. Beiu: A Novel Highly Reliable Low-Power Nano Architecture –
When von Neumann Augments Kolmogorov
IEEE International Conference on Application-specific Systems, Architectures and Processors ASAP'04
Galveston, TX, USA, September 27-29, 2004

P_{45} J. Nyathi, V. Beiu, and S. Aunet
Femto Joule Switching — Review of Low Energy Design Styles for the Nano Era
International Symposium on Nano and Giga Challenges in Nanoelectronics NGCM'04
Krakow, Poland, September 13-17, 2004

P_{44} V. Beiu, J.M. Quintana, M.J. Avedillo, and M.H. Sulieman: Threshold Logic – From TTL to Nanoelectronics
IEEE International Midwest Symposium on Circuit and Systems MWSCAS'03
Cairo, Egypt, December 27-30, 2003

P_{43} M.H. Sulieman, and V. Beiu: Review of Recent Full Adders Implemented in Single Electron Technology
IEEE International Midwest Symposium on Circuit and Systems MWSCAS'03
Cairo, Egypt, December 27-30, 2003

P_{42} S. Roy, V. Beiu, and M.H. Sulieman: Reliability Analysis of Some Nano Architectures
Neural Information Processing System NIPS'03, Whistler, Canada, December 12-13, 2003

P_{41} J.M. Quintana, M.J. Avedillo, and V. Beiu: Beyond Threshold Logic Gates
Neural Information Processing System NIPS'03, Whistler, Canada, December 12-13, 2003

P_{40} M.H. Sulieman, and V. Beiu: Characterization of Optimal Practical Adders for SET
Neural Information Processing System NIPS'03, Whistler, Canada, December 12-13, 2003

P_{39} J. Nyathi, V. Beiu, S. Tatapudi, and D.J. Betowski: Low Power Charge Recycling Asynchronous Designs
Neural Information Processing System NIPS'03, Whistler, Canada, December 12-13, 2003

P_{38} V. Beiu: Threshold Logic – From the Early Days into the Nanoera
Neural Information Processing System NIPS'03, Whistler, Canada, December 12-13, 2003

P_{37} V. Beiu: Review of Silicon Nanoelectronics and Beyond
Neural Information Processing System NIPS'03, Whistler, Canada, December 12-13, 2003

P_{36} V. Beiu: Designing with Perceptrons
University of Paderborn, Paderborn, Germany, November 10, 2003

P_{35} V. Beiu: Advanced Real-Time-Radiography Graphical Object Selection (ARGOS)
Washington State University, Pullman, WA, USA, October 11, 2002

P_{34} V. Beiu, H.E. Makaruk, D. Morgan, and L. Popa-Simil
ARGOS – Advanced RTR Graphical Object Selection
Los Alamos National Laboratory, Los Alamos, NM, USA, July 24, 2002

$P_{23\text{-}33}$ V. Beiu: On VLSI-Optimal Neural Computations
– University of Hawaii, Honolulu, HI, USA, April 12, 2001
– Rutgers University, Rutgers, NJ, USA, April 9, 2001
– Boston University, Boston, MA, USA, April 6, 2001
– University of Texas at Arlington, Arlington, TX, USA, April 2, 2001
– Rochester Institute of Technology, Rochester, NY, USA, March 22, 2001
– California Polytechnic State University, San Luis Obispo, CA, USA, March 19, 2001
– University of Wisconsin Milwaukee, Milwaukee, WI, USA, March 9, 2001
– University of California at Riverside, Riverside, CA, USA, March 2, 2001
– Illinois Institute of Technology, Chicago, IL, USA, February 23, 2001
– Washington State University, Pullman, WA, USA, February 9, 2001
– Metroplex Institute for Neural Dynamics (MIND), Dallas, TX, USA, November 4, 2000

P_{22} V. Beiu: On Biological and Hardware Neural Networks
International Joint Meeting AMS-SMM, Denton, TX, USA, May 19-22, 1999

P_{21} V. Beiu: A Novel Microsatellite Control System
International ICSC Symposium on Engineering of Intelligent Systems EIS'98
Tenerife, Canary Islands, Spain, February 9-13, 1998

P_{20} V. Beiu: A Space-Based Radio Frequency Transient Event Classifier
International ICSC Symposium on Engineering of Intelligent Systems EIS'98
Tenerife, Canary Islands, Spain, February 9-13, 1998

P_{19} V. Beiu: On VLSI-Optimal Constructive Algorithms for Classification Problems
International ICSC Symposium on Engineering of Intelligent Systems EIS'98
Tenerife, Canary Islands, Spain, February 9-13, 1998

P_{18} V. Beiu: Time-Space Trade-Offs in Parallel and Neural Computing
International ICSC Symposium on Engineering of Intelligent Systems EIS'98
Tenerife, Canary Islands, Spain, February 9-13, 1998

P_{17} V. Beiu, and H.E. Makaruk: Deeper and Sparser Nets Are Optimal
International ICSC Symposium on Engineering of Intelligent Systems EIS'98
Tenerife, Canary Islands, Spain, February 9-13, 1998

P_{16} R. Andonie, and V. Beiu: Optimization of Circuits Using Neural Networks
Workshop on Shaping the Hardware Solutions for the Third Millennium ANITA'96
Uppsala, Sweden, December 9-10, 1996

P_{15} V. Beiu: VLSI Complexity of Threshold Gate COMPARISON
International Symposium on Neuro-Fuzzy Systems AT'96
Lausanne, Switzerland, August 29-31, 1996

P_{14} V. Beiu, and J.G. Taylor: Area-Efficient Constructive Learning Algorithm
International Conference on Control System and Computer Science CSCS-10
Bucharest, Romania, May 25, 1995

P_{13} V. Beiu: Optimal VLSI Implementations of Neural Networks – VLSI-Friendly Learning Algorithms
Applied Decision Technologies Conference ADT'95, London, UK, April 3-5, 1995

P_{12} V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Addition Using Constrained Threshold Gates

International Conference on Technical Informatics ConTI'94
Timişoara, Romania, November 16-19, 1994

P_{11} V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Digital Implementations of Neural Networks Using Threshold Gates
International Conference Romania and Romanians in Contemporary Science RRCS'94
Sinaia, Romania, May 24-27, 1994

P_{10} V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
VLSI Complexity Reduction by Piece-Wise Approximation of the Sigmoid Function
European Symposium on Artificial Neural Networks ESANN'94, Brussels, Belgium, April 20-22, 1994

P_9 V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Learning from Examples and VLSI Implementation of Neural Networks
European Meeting on Cybernetics and System Research EMCSR'94, Vienna, Austria, April 5-8, 1994

P_8 V. Beiu: J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Close Approximations of Sigmoid Functions by Sum of Steps
Romanian Symposium on Computer Science ROSYCS'93, Iaşi, Romania, November 12-13, 1993

P_7 V. Beiu, J.A. Peperstraete, J. Vandewalle, and R. Lauwereins
Overview of Some Efficient Threshold Gate Decomposition Algorithms
International Conference on Control System and Computer Science CSCS-9
Bucharest, Romania, May 25-28, 1993

P_6 V. Beiu, J.A. Peperstraete, and R. Lauwereins: Enhanced Threshold Gate Fan-in Reduction Algorithm
Interdisciplinary Centrum for Neural Networks ICNN'92, Leuven, Belgium, November 19, 1992

P_5 V. Beiu: D. C. Ioan, M. Dumbrava, and O. Robciuc
Physical Fields Determination Using Continuous Boltzmann Machines
Symposium on Parallel Computing SPC'91, Bucharest, Romania, December 10-11, 1991

P_4 V. Beiu: Neural Network Priority Queue
International Workshop on Parallel Processing by Cellular Automata PARCELLA'90
Berlin, Germany, September 19-21, 1990

P_3 V. Beiu: From Systolic Arrays to Neural Networks
International Symposium on Informatics INFO-IASI'89, Iaşi, Romania, October 19-21, 1989

P_2 V. Beiu: Memory Structure with Simultaneous Read and Write Capabilities
Conference of the Military Academy of Sciences, Bucharest, Romania, November 17-19, 1982

P_1 V. Beiu: Reliability Enhanced Memory Architecture with Gracefully Degrading Performances
Jubilee Session: Ten Years from the Foundation of the Special High-School for Informatics
Bucharest, Romania, May 1981

46 invited presentations (to industry)

I_{46} T.-J. King Liu, V. Beiu, M. Tache, W. Ibrahim, and A. Beg
Ultra Low Power Hybrid NEMS-CMOS
SRC GRC SLD Design Review, Intel, Hillsboro, OR, USA, May 7, 2015

I_{45} V. Beiu, G. Fettweis, M. Alioto, F. Kharbash, and W. Ibrahim
Technical Mapping onto FinFETs
SRC GRC ACE4S Annual Review, Abu Dhabi, UAE, April 23, 2014

I_{44} V. Beiu, T.-J. King Liu, G. Fettweis, M. Alioto, F. Kharbash, W. Ibrahim, A. Beg, and M. Tache
Ultra-low Power: Unconventional Sizing, NEMS, and FinFETs
SRC GRC Design Review, Bangalore, India, January 10, 2014

I_{43} V. Beiu, T.-J. King Liu, W. Ibrahim, A. Beg, and M. Tache
Ultra Low Power Hybrid NEMS-CMOS
SRC GRC ICSS Circuits and Texas Analog Center of Excellence (TxACE)
UT Dallas, Dallas, TX, USA, October 25, 2013

I_{42} V. Beiu, M. Alioto, A. Beg, W. Ibrahim, and F. Kharbash
Unconventional Sizing for Enabling Low Power Digital Design
SRC GRC CADTS LPD, Georgia Tech, Atlanta, GA, USA, October 2, 2013

I_{41} V. Beiu, G. Fettweis, M. Alioto, F. Kharbash, and W. Ibrahim
Ultra-low Power Digital FinFET Amplifiers
SRC/ATIC ACE4S Kickoff Meeting, Abu Dhabi, UAE, September 23, 2013

I_{40} V. Beiu, T.-J. King Liu, W. Ibrahim, A. Beg, and M. Tache
Ultra Low Power Hybrid NEMS-CMOS
SRC GRC ICSS Circuits and Texas Analog Center of Excellence (TxACE)
UT Dallas, Dallas, TX, USA, October 25, 2012

I_{39} V. Beiu, M. Alioto, A. Beg, W. Ibrahim, and F. Kharbash
Unconventional Sizing for Enabling Low Power Digital Design
SRC-MEES Kickoff Meeting, Abu Dhabi, UAE, October 21, 2012

I_{38} V. Beiu, T.-J. King Liu, W. Ibrahim, A. Beg, and M. Tache
Ultra Low Power Hybrid NEMS-CMOS
SRC-MEES, Abu Dhabi, UAE, October 21, 2012

I_{37} V. Beiu, W. Ibrahim, A. Beg, and F. Kharbash
Ultra Low Power Hybrid NEMS-CMOS
IBM-CIT, UAEU, Al Ain, UAE, October 4, 2012

I_{36} V. Beiu: On the Reliability Accuracy Challenge − Bio-inspired Arrays to the Rescue
Intel, Portland, OR, USA, March 29, 2012

I_{35} V. Beiu, T.-J. King Liu, W. Ibrahim, A. Beg, and M. Tache: Ultra Low Power Hybrid NEMS-CMOS
SRC-MEES Kickoff Meeting for New ATIC Projects (web-conference), NC, USA, January 17, 2012

I_{34} V. Beiu: On the Reliability of Self-assembled 2D and 3D Arrays
Intel, Santa Clara, CA, USA, November 17, 2011

I_{33} V. Beiu, T.-J. King Liu, W. Ibrahim, and A. Beg: Ultra Low Power Hybrid NEMS-CMOS
SRC/ATIC University Research Kickoff Meeting
Abu Dhabi, UAE, October 26, 2011

I_{32} V. Beiu: Brain-inspired Hybrid Topologies for Nano-architectures
SRC GRC ICSS Circuits and Texas Analog Center of Excellence (TxACE)
UT Dallas, Dallas, TX, USA, October 24-28, 2011

I_{31} V. Beiu: From Reliable Neurons to Regular Nano-Fabrics — Six Month Later
Intel, Santa Clara, CA, USA, February 25, 2011

I_{30} V. Beiu: From Reliable Neurons to Regular Nano-Fabrics
Intel, Santa Clara, CA, USA, September 9, 2010

I_{29} V. Beiu: Reliable Ultra Low-Power Information Processing
ATIC (http://www.atic.ae/, now Mubadala Technology) Abu Dhabi, UAE, March 2010

I_{28} V. Beiu: When Electrons Start Showing Their True Colors — Quo Vadis Nanoarchitectures?
IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA, June 2008

I_{27} V. Beiu: Brain Inspired Nano Architectures — Electrons Behaving Badly
IBM Research, Böblingen, Germany, May 20, 2008

I_{26} V. Beiu: Interconnect Tyranny – Brain's versus Rent's Rule
HP Labs, Santa Clara, CA, USA, April 26, 2007

I_{25} V. Beiu: On 3D Nano-Designs – In the Yield-Energy-Delay Realm
International Technology Roadmap for Semiconductors (ITRS), SRC, Austin, TX, USA, March 22, 2007

$I_{20\text{-}24}$ V. Beiu: On Neural-Inspired Nano Architectures (CNINA)
– Synplicity, September 26, 2003
– AMD, September 26, 2003
– Agilent Labs, September 25, 2003
– Infineon, September 25, 2003
– SUN Microsystems, September 25, 2003

$I_{18\text{-}19}$ G. LaRue, V. Beiu, and F. Shi
Direct Digital Frequency Synthesizer for Reconfigurable Communication Systems
– Air Force Research Laboratory (AFRL) and the Centre for Design of Analog-Digital ICs (CDADIC)
Welches, OR, USA, July 9-11, 2003
– Air Force Research Laboratory (AFRL) and the Centre for Design of Analog-Digital ICs (CDADIC)
Seattle, WA, USA, February 7, 2003

I_{17} V. Beiu: Direct Digital Frequency Synthesizers: A Survey
Boeing, Seattle, WA, USA, February 5, 2003

I_{16} G. La Rue, V. Beiu, and F. Shi: Direct Digital Frequency Synthesizer for Reconfigurable Communication Systems
Air Force Research Laboratory (AFRL) and the Centre for Design of Analog-Digital ICs (CDADIC)
Stevenson, Washington, USA), July 10, 2002

$I_{1\text{-}15}$ V. Beiu: ... (under NDAs)
– Q'Bit Systems SRL, Bucharest, Romania, October 24, 2000
– ESSEX Com SRL, Bucharest, Romania, October 23, 2000
– Utimaco, Brussels, Belgium, May 26, 2000
– ST Microelectronics, San Diego, CA, USA, September 29, 1999
– ST Microelectronics, Carrollton, TX, USA, August 20, 1999
– Texas Instruments, Dallas, TX, USA, August 16, 1999
– Sipex, Milpitas, CA, USA, August 13, 1999
– ST Microelectronics, San Jose, CA, USA, August 13, 1999

– ST Microelectronics, San Jose, CA, USA, April 16, 1999
– National Semiconductors, Santa Clara, CA, USA, April 16, 1999
– Alcatel, Bruxelles, Belgium, April 14, 1999
– Texas Instruments, Dallas, TX, USA, April 1, 1999
– Texas Instruments, Houston, TX, USA, March 25, 1999
– Metaflow, La Jolla, CA, USA, February 18, 1999
– Texas Instruments, Houston, TX, USA, September 21, 1998

Research projects

PI on **28** **research grants/contracts** **9.6M US$**

2016-2019	– Novel Bio-inspired Cellular Nano-Architectures (BioCell-NanoART), POC-A1-A1.1.3-E-2015 With V.-F. Duma (UAV), F.-D. Munteanu (UAV), V.E. Bălaş (UAV), M. Bălaş (UAV), and O.P. Gaşpar (UAV)	8.5M RON
2014-2015	– Ultra-low Power Digital Sub-threshold FinFET Amplifiers (ULP-DigiFinA), SRC GRC ACE4S With F. Kharbash (UAEU), and W. Ibrahim (UAEU)	120K$
2011-2015	– Ultra Low Power NEMS-CMOS (ULP-NEMS-CMOS) SRC 2011-HJ-2184 With T.-J.K. Liu (UC Berkeley), W. Ibrahim (UAEU), and A. Beg (UAEU)	300K$
2012-2014	– Unconventional Sizing for Enabling Low Power Digital Design (Use-LP), SRC 2012-TJ-2332 With M. Alioto (U Siena / Natl. U Singapore), A. Beg (UAEU), W. Ibrahim (UAEU), and F. Kharbash (UAEU)	200K$
2011-2013	– Brain-inspired Interconnects for Nanoelectronics (BiIN) NRF 1108-00451 With W. Ibrahim (UAEU)	160K$
2011-2012	– Brain-inspired Hybrid Topologies for Nano-architectures SRC 2011-RJ-2150G	40K$
2009-2011	– Brain-inspired Interconnects for Nanoelectronics British Council PMI2 RCGS271	39K£
2000-2003	– Ultra-fast Low-power FPUs for Graphics and Gaming Rose Research	500K$
2000-2003	– Ultra-fast Low-power En/decryption for Wire-speed Crypto-processors Rose Research	500K$
1999-2005	– FastLogic (enabling VLSI based on novel ultra-fast logic gates) Rose Research	3M$
1999-2002	– Ultra-fast Low-power Multiplication & Multiply-accumulate for DSP Rose Research	1M$
1998-1999	– Enhanced Ultra-fast VLSI Adders Rose Research	500K$
1996-1998	– Field Programmable Neural Arrays, Los Alamos Natl. Laboratory	180K$
1994-1996	– Programmable Neural Arrays for Implementing Neural Networks EU CHBICT941741	440K$
1990-1991	– Dedicated En/Decryption and GUI, Ministry of National Defense	20K$
1990-1991	– Computer Aided Designing, Aversa SA	5K$
1990-1991	– Data Acquisition CAD Package, Chemistry Research Inst.	10K$
1990-1991	– Dedicated/Custom Software Package, Ministry of National Defense	5K$
1988	– Dedicated Watch-dog System, Electrical Networks Institute	50K$
1987	– Dedicated Database Package National Institute for Information & Documentation	50K$

1987	– Hierarchical Self-testable/-repairable Content Addressable Memory UPBucharest	50K$
1987	– High Speed Antialiasing Cascadable Circuit, UPBucharest	50K$
1985-1987	– VLSI CAD Package, UPBucharest	100K$
1984-1986	– Automatic Conical Ball Bearing Sorter, Rulmentul Alexandria	100K$
1983	– Mutual exclusion circuit (patented), ITC/CCAB	
1981-1982	– Ultra high-speed FPU, ITC/CCA	
1981	– Ultra high-speed highly reliable CPU, ITC/CCA	
1979-1980	– High speed (60MHz) graphic workstation (1024×1024), UPBucharest	5K$

Co-PI on 16 research grants/contracts **42M US$**

2013-2016	– Strengthening Research Collaborations in High-impact & Emerging Technologies between GCC and EU (SECRET) EU EM 545790-EM-1-2013-1-UK-ERA MUNDUS-EMA22 With B. Aziz M. Rahman PI (City U London), G. Cuniberti (TU Dresden), V. Hessel (TU Eindhoven), O. Benitez (U Deusto), P. Candeloro (U Magna Graecia), C. Themistos (Frederick U), H. Bourdoucen (Sultan Qaboos U), F. Bou-Rabee (Kuwait U), S.A. Al-Mansoori (U Bahrain), F. Kharbash (UAEU)	1.2M€
2011-...	– Ultra Low-Power Application-specific Non-Boolean Architectures (ULP-NBA), URO 2011-05-24G With Intel PI, D. Hammerstrom (Portland State U), W. Porod (U Notre Dame), S.P. Levitan (U Pittsburgh), T. Shibata (U Tokyo), T. Roska (Hungarian Acad. Sci.), M. Pufall (NIST), D. Weistein (MIT), and M.R. Stan (U Virginia)	1M$
2012-2015	– Synaptic Molecular Networks for Bio-inspired Information Processing EU FP7-ICT-318597 With G. Wendin PI (Chalmers U), D. Vuillaume (CNRS-IEMN), J. Roncali (CNRS-MOLTECH), M. Calame (Basel U), S. Yitzchaik (HUJI), C. Gamrat (CEA), and G. Cuniberti (TU Dresden)	2.8M€
2011-2013	– Algorithms & EDA for Accurate Nano-Circuits Reliability Calculations NRF 1108-00329 With W. Ibrahim PI (UAEU)	138K$
2009-	– Emirates Center for Nanoscience & Nanoengineering (on hold) http://www.thenational.ae/news/uae-news/education/grant-aids-research-centres With Yousef Haik PI (UAEU) et al.	13.6M$
2007-2010	– Center for Neural Inspired Nano Architectures, Univ. Ulster With M. McGinnity PI (UUlster) et al.	1.8M£
2007	– Mapping the Proxel Method to Reliability Analysis of Nanoarchitectures UAEU With S. Lazarova-Molnar PI (UAEU)	2.2K$
2006-...	– Center for Excellence in Intelligent Systems, InvestNI & IDF With M. McGinnity PI (UUlster) et al.	20.4M£
2006	– Investigation of the Reliability of SET Gates & Circuits, UAEU With M.H. Sulieman PI (UAEU)	2.2K$
2005-2006	– Defect-tolerant high-perf. low-power computing with hybrid CMOL, ARDA With K.K. Likharev PI (Stony Brook U) et al.	100K$
2002-2004	– DDFSys for reconfigurable communication system, AFRL With G LaRue PI (WSU)	250K$
1992-1994	– VLSI-efficient threshold logic gates Concerted Research Action of the Flemish Community With J. Vandewalle PI (KULeuven) et al.	20K$

1990-1991	– Software Package for Microbusiness National Institute for Research & Development in Chemistry With A. Florea (UPBucharest)	10K$
1987-1988	– Studied and Analyzed Prolog as a Tool for Circuit Simulations UPBucharest With V. Ivanov PI (UPBucharest)	
1983	– Floppy disk interface, ITC/CCAB	
1980	– Testing of the CE-100 computer, ITC/CCAB	

PI on **93** short-term travel grants **225K US$**

1987	CompEuro'87	Hamburg, Germany	0.4K$
1990	PARCELLA'90	Berlin, Germany	0.3K$
1991	ICANN'91	Espoo, Finland	1.5K$
	ICIAM'91	Washington, DC, USA	1.5K$
1992	EPFLausanne	Lausanne, Switzerland	0.5K$
1993	ESSAN'93	Brussels, Belgium	0.6K$
	ROSYCS'93	Iassy, Romania	0.3K$
1994	RRCS'94	Sinaia, Romania	0.5K$
	EMCSR'94	Vienna, Austria	0.3K$
	ConTI'94	Timisoara, Romania	0.3K$
1995	ADT'95	London, UK	0.5K$
1996	AT'96	Lausanne,Switzerland	0.5K$
	SBRN'96	Recife, Brazil	2.5K$
	ANITA'96	Uppsala, Sweden	1.5K$
1997	NEuroTop'97	Brasov, Romania	0.5K$
	Oxford Univ.	Oxford, UK	1K$
	Royal Holloway Univ.	Egham, UK	1K$
	Univ. Paris XII	Paris, France	1K$
	Heinz Nixdorf Inst.	Paderborn, Germany	1.5K$
	IDIAP Res. Inst.	Martigny, Switzerland	2K$
	SBRN'97	Goiania, Brazil	5K$
1998	EIS'98	Tenerife, Spain	1K$
	PARELEC'98	Bialystok, Poland	0.5K$
	CNRS	Paris, France	1K$
	NC'98	Vienna, Austria	0.5K$
1999	AMS-SMM'99	Denton, TX, USA	0.5K$
2001	UCBerkeley Wireless Res. Center	Berkeley, CA, USA	4K$
2002	Los Alamos Natl. Lab	Los Alamos, NM,USA	5K$
2003	Heinz Nixdorf Inst.	Paderborn, Germany	2K$
	NCI'03	Cancun, Mexico	0.5K$
	IWANN'03	Menorca, Spain	0.5K$
	IJCNN'03	Portland, OR, USA	0.5K$
	Univ. Paderborn	Paderborn, Germany	1.5K$
	NIPS'03	Whistler, Canada	0.5K$
	ICNNSP'03	Nanjing, China	0.5K$
	MWSCAS'03	Cairo, Egypt	0.5K$
2004	Heinz Nixdorf Inst.	Paderborn, Germany	1.5K$
	IJCNN'04	Budapest, Hungary	0.5K$
	NGCM'04	Krakow, Poland	1K$
	ASAP'04	Galveston, TX, USA	0.5K$

2005	IIT'05	Dubai, UAE	1K$
	NSF-SRC SNB'05	Portland, OR, USA	3K$
	Univ. Ulster	Londonderry, UK	9K$
	ICM'05	Islamabad, Pakistan	3K$
2006	AICCSA'06	Sharjah, UAE	0.5K$
	IDT'06	Washington, DC, USA	0.5K$
	WNEC'06	Mumbai, India	2.5K$
	NSF	Washington, DC, USA	5K$
2007	Univ. Oslo	Oslo, Norway	5K$
	NanoMaterials'07	San Diego, CA, USA	0.5K$
	IWANN'07	San Sebastián, Spain	5K$
	IDT'07	Cairo, Egypt	0.5K$
	ICTRF'07	Abu Dhabi, UAE	0.5K$
	ICSPC'07	Dubai, UAE	0.5K$
	IEEE-NANO'07	Hong Kong, China	1K$
	MWSCAS'07	Montreal, Canada	1K$
	Tohoku Univ.	Sendai, Japan	5K$
	IECON'07	Taipei, Taiwan	3K$
	DCIS'07	Seville, Spain	3K$
	DTIS'07	Rabat, Morocco	3K$
	SHARCS	London,UK	2K$
	ISMVL'07	Oslo, Norway	1K$
	ULSIWS'07	Oslo, Norway	0.4K$
	FENA/UCLA	Los Angeles, CA, USA	1K$
	HP Labs	Palo Alto, CA, USA	6K$
	EU	Brussels, Belgium	8K$
	NSF	Washington, DC, USA	5K$
2008	Univ. Oslo	Oslo, Norway	5K$
	Univ. Paris-Sud	Paris, France	3K$
	Tohoku Univ.	Sendai, Japan	10K$
	SAMOS'08	Samos, Greece	5K$
	Los Alamos Natl. Lab	Los Alamos, NM, USA	2K$
	NSF	Washington, DC, USA	5K$
2009	WDSN'09	Estoril/Lisbon, Portugal	5K$
	NanoNet'09	Luzern, Switzerland	1K$
	ESSCIRC'09	Athens, Greece	1.5K$
	IEEE- NANO'09	Genoa, Italy	1K$
	Univ. Oslo	Oslo, Norway	5K$
	EU	Cambridge, UK	7K$
2010	MEES'10	Abu Dhabi, UAE	3K$
	INC6	Grenoble, France	1K$
	IJCNN'10	Barcelona, Spain	1.5K$
	IDT'10	Abu Dhabi, UAE	0.5K$
2011	ATIC-SRC	Abu Dhabi, UAE	10K$
	NSF	Washington, DC, USA	5K$
	EU	Paris, France	5K$
	EU	Brussels, Belgium	8K$
	IEEE-NANO'11	Portland, OR, USA	0.5K$
2012	EDCC'12	Sibiu, Romania	1K$
2013	TUDresden	Dresden, Germany	7K$
2016	ICCCC'16	Oradea, Romania	0.5K$
	SOFA'16	Arad, Romania	pending
	TUDresden	Dresden, Germany	pending
	IEEE-NANO'16	Sendai, Japan	pending

Conferences **List of conferences organized and sessions chaired**

110 organized

RRCS'94, ANITA'96, NEuroFuzzy'96, NeuroTop'97, SBRN'97, EIS'98, SOCO'99, EIS'00, SBRN'00, IWANN'03, NCI'03, IJCNN'04, IJCNN'05, NanoArch'05, IDT'06, IEEE-NANO'06, IEEE SoC'06, IJCNN'06, NanoArch'06, WSC-11, ICMENS'06, IDT'07, IIT'07, IEEE SoC'07, IJCNN'07, MCSoC'07, NanoArch'07, WSC-12, DCS'08, IDT'08, MIM-MMN'08, NanoArch'08, NDCS'08, VTS'08, WSC-13, DTIS'09, ICMLA'09, IJCNN'09, MIM-MMN'09, NanoArch'09, NanoNet'09, WSC-14, BCN'10, BIONETICS'10, ICTITA'10, IDT'10, MIM-MMN'10, MCSoC'10, NanoArch'10, NaNoNet'10, SBCCI'10, WAC'10, WSC-15, ICMLA'11, IDT'11, MIM-MMN'11, MoNaCom'11, NaBIC'11, NanoArch'11, SBCCI'11, ISIE'12, MIM-MMN'12, MoNaCom'12, NaBIC'12, NanoArch'12, OPTIM'12, SBCCI'12, WICT'12, WSC-16, DTIS'13, ICECS'13 (track chair), IDT'13, IIT'13, IJCNN'13, MIM-MMN'13, MoNaCom'13, NanoArch'13, SBCCI'13, VLSI-SoC'13, BICT'14, BioTL'14, DTIS'14, I4CT'14, ICECS'14 (track chair), ICNC'14, IIT'14 (chair), IDT'14, ISCAS'14, MIM-MMN'14, NanoArch'14, NanoCom'14, SBCCI'14, SSCI'14, DTIS'15, ECCTD'15, ICECS'15 (track chair), IDT'15, IJCNN'15, MIM-MMN'15, NaBIC'15, NanoArch'15, NanoCom'15, SBCCI'15, SSCI'15, DTIS'16, ICCCC'16, ICECS'16 (publicity chair), ISCAS'16, MIM-MMN'16, SETIT'16

57 sessions chaired

CSCS'93, ROSYCS'93, RRCS'94, ConTI'94, ADT'95, CSCS'95, IWANN'95, NeuroTop'97, CSCS'97, EANN'97, SOCO'97, EIS'98 (2 sessions), PARELEC'98, NC'98, ISCAS'00, MWSCAS'00 (2 sessions), NCI'03 (2 sessions), IWANN'03, ICANN'03, SCS'03, IJCNN'03, NIPS'03 (2 sessions), MWSCAS'03, IJCNN'04 (2 sessions), IJCNN'05, IIT'05, VLSI-SoC'05, ICM'05, AICCSA'06 (2 sessions), IIT'06, ISMVL'07, IWANN'07, IEEE-NANO'07, DCIS'07, GCoE'07, ARC'08, GCoE'08, ISCAS'08, ARC'09, NanoNet'09, IDT'10, IEEE-NANO'11, EDCC'12, IEEE-NANO'12, DTIS'13, ICECS'13 (3 sessions), IIT'14, ICCCC'16

Sessions / Workshops **10 invited sessions/workshops organized**

S_{10}	R. Andonie, D. Davendra, and V. Beiu: Computational Intelligence Methods IEEE International Conference on Computers, Communications and Control ICCCC'16 Baile Felix, Oradea, Romania, May 10-14, 2016	Session
S_9	V. Beiu, and W. Ibrahim: Towards Brain Inspired Interconnects and Circuits International ICST Conference on Nano-Networks Nano-Net'09 Luzern, Switzerland, October 18, 2009	Workshop
S_8	M.J. Avedillo, J.M. Quintana, and V. Beiu Emerging Technologies Applied to Nanoelectronics IEEE International Conference on Design of Circuits and Integrated Systems DCIS'07 Seville, Spain, November 22, 2007	Session
S_7	U. Rückert, and V. Beiu: Neural Inspired Architectures for Nanoelectronics International Work-Conference on Artificial Neural Networks IWANN'07 San Sebastian, Spain, May 19, 2007	Session
S_6	V. Beiu, and U. Rückert Brain Inspired Emerging Nanoarchitectural Design and Technical Challenges IEEE International Joint Conference on Neural Networks IJCNN'04 Budapest, Hungary, July 28, 2004	Session
S_5	V. Beiu, and U. Rückert: Neural-inspired Architectures for Nanoelectronics Neural Information Processing Systems NIPS'03 Whistler, Canada, December 12-13, 2003	Workshop
S_4	V. Beiu: Threshold Gates – Past, Present, and Future International Work-Conference on Artificial Neural Networks IWANN'03 Menorca, Spain, June 4, 2003	Session
S_3	V. Beiu: The Next Generation of Neural Networks Chips Session International ICSC Symposium on Engineering of Intelligent Systems EIS'98 Tenerife, Spain, February 9, 1998	Session
S_2	R. Andonie, and V. Beiu International Workshop on Neural Research Priorities NeuroTop'97 Braşov, Romania, May 27-28, 1997	Workshop
S1	V. Beiu, and R. Andonie: Shaping the Hardware Solutions for the Third Millennium ANITA'96 Uppsala, Sweden, December 9-10, 1996	Workshop

Courses	Taught and developed	Since	UPB	WSU	UAEU	UAV
Undergraduate	– Hardware Testing & Fault Tolerance	2013			UAEU	
	– Professional Responsibility in IT	2012			UAEU	
	– Advanced Computer Architecture	2006			UAEU	
	– ASIC & Digital Systems / VLSI Design	2001		WSU	UAEU	
	– Introduction to Programming	1984	UPB			
	– Digital Computer Architecture	1983	UPB		UAEU	
	– Analysis & Synthesis of Digital Circuits	1981	UPB		UAEU	
Graduate	– Neuro-Bio Fundamentals	2015				UAV
	– Research Methods in IT	2011			UAEU	
	– Advanced VLSI / Nanoelectronics	2004		WSU		
	– Neural Computations	2003		WSU		UAV
	– Neural Networks & Applications	1990	UPB	WSU		
	– VLSI Design & Applications	1983	UPB			UAV
	– Advanced Computer Architecture	1983	UPB			
	– Testing & Performance Evaluation	1982	UPB			

Graduate Supervision UAEU (1), BITS (2), WSU (3), UPB (29)

2013	35	– Monte Carlo Analyses of XOR-2 in 22/16nm PTM	Nilay V. Acharya	MSc
	34	– Monte Carlo Analyses of MAJ-3 in 22/16nm PTM	Jithu Lissi Raju	MSc
2012	33	– Brain-inspired Interconnects for Nanoelectronics	Pietro Santagati	PostDoc
2004	32	– Design & Analysis of SET: Neural-Inspired Gates & Circuits	Mawahib H. Sulieman	PhD
	31	– Optimizing the Performance of Direct Digital Frequency Synthesizers for Low-Power Wireless Communication	David Betowski	MSc
2003	30	– Precise Sine Approximations with Reduced Resources	Pao-Szu Wu	MSc
1991	29	– Simulator for the Implied Minterm Structure	Simona Ivanov	MSc
1990	28	– Set of C Functions for Simulating Parallel Processes	Dinu Creteanu	MSc
	27	– Graphic Interface for a Neural Network Simulator	Dan Stoicescu	MSc
	26	– Microbusiness Software Package	Anca Costin	MSc
	25	– Neural Network Arithmetic Logic Unit	Yousuf Basmark	MSc
	24	– VLSI Parallel Architecture for Histogram Modification	Aida Gheorghiu	MSc
	23	– Boltzmann Machine Simulator	Mihaela Dumbrava	MSc
	22	– Neural Network Solutions to Optimization Problems	Orest Robciuc	MSc
	21	– Motion Detection Using Neural Networks	Anca Sigala	MSc
	20	– Enhanced VLSI CAD Package	Daniel Mandu	MSc
1989	19	– Recognition of Characters Using Neural Networks	Abdel Nehad	MSc
	18	– Neural Network Medical Expert System	Sima Gheorghita	MSc
	17	– VLSI Animated Lesson for PC	Şerban Benone	MSc
1988	16	– Neural Network Simulator	Sobhui Darwish	MSc
1987	15	– VLSI CAD Tool: Place & Route	Anca Şerban	MSc
	14	– VLSI CAD Tool: Interactive Layout	Mariana Mirea	MSc
1986	13	– Computer Interface for a Rotating Magnetic Head Unit	Sorinel Ciobanu	MSc
	12	– CAD Tool for Digital Image Segmentation	Cornelia Ciotînga	MSc
	11	– CAD Tool for Digital Image Enhancement	Mihai Dinu	MSc
1985	10	– Systolic Floating Point Coprocessor: Multiplication & Division	Eugen Paşol	MSc
	9	– Systolic Floating Point Coprocessor: Addition & Subtraction	Liviu Zuzu	MSc
	8	– VLSI Ultra High-Speed Arithmetic Units	Marius Ionescu	MSc
	7	– Dedicated Serial Data Multiplier	Daniel Manica	MSc
	6	– Systolic Circuits for Convolution	Anca Tanga	MSc
	5	– A Study of Permutation Networks for VLSI Implementation	Sorin Tene	MSc
1984	4	– VLSI Rule Checking Expert System	Manuela Anton	MSc
	3	– High Speed Arithmetic Units	Bianca Tudor	MSc
	2	– Self-Testable RAM/CAM Memory	Cristina Borş	MSc
	1	– Self-Testable & Self-Repairable Correlation Circuit	Irina Manole	MSc

Service

2013 – 2015	University Promotion Advisory Group	Member
2009 – 2015	University Mubadala Technology (previously ATIC) Advisory Board	Member
2013 – 2015	Faculty Promotion Committee	Chair
2005 – 2013	Faculty Promotion Committee (except 2007 – 2008)	Member
2014 – 2015	Faculty Peer Evaluation of Teaching (PET) Committee	Member
2010 – 2013	University Council	Member
2008 – 2013	University Graduate Research Studies Board	Member
2008 – 2011	University Graduate Council	Member
2007 – 2009	University Technical Task Force	Member
2006 – 2010	University Research Affairs Committee	Member
2006 – 2007	University IT Receiving Committee	Member
2011 – 2013	Faculty Research Committee	Member
2011 – 2012	Faculty Graduate Program Committee	Member
2009 – 2011	Faculty Graduate Program Committee	Chair
2005 – 2011	Faculty Research & Graduate Studies Committee	Chair
2005 – 2008	Faculty Laboratories & Equipment Committee	Chair
2005 – 2006	Faculty Recruitment Committee	Chair
2006 – 2011	Faculty Strategic Planning Committee	Member
2006 – 2010	Faculty Recruitment Committee	Member
2006 – 2009	Faculty Honors Committee	Member
2006 – 2007	Faculty Academic Performance Assessment Committee	Member
2005 – 2011	Faculty Council	Member
2005 – 2008	Faculty Curriculum Committee	Member

2006 –	Established and leading Nano-ART = Nano Architectural Research Team
2009	External examiner for one PhD thesis (member of the examination committee)
2008	External examiner for four PhD theses (member of the examination committee)
2007	External examiner for one PhD thesis (member of the examination committee)
	External examiner HCT Men's College, Abu Dhabi (9 students, 4 projects)
2006	External examiner for one PhD thesis (member of the examination committee)
2005	External examiner for one PhD thesis (member of the examination committee)

2001 – 2005	Faculty Graduate Studies Committee	Member
2001 – 2005	Computer Engineering (Program) Committee	Member
1998 – 2001	International Computer Science Conventions / Academic Advisory Board	Member
1997 – 1998	Program Chairman of the IEEE Los Alamos Section	Chair
1985 – 1990	Secretary of the MSc Examination Board	
1987 July	Chair of the Students' National Computer Training Camp (Sinaia, Romania)	Chair
1985 – 1990	Chair of the Students' Group for Scientific Computer Research	Chair

2011 – 2015	Associate Editor IEEE Transactions on VLSI Systems	IEEE
2010 –	Associate Editor Nano Communication Networks	Elsevier
2009 –	Emerging Technologies Group on Nanoscale Communications	IEEE
2005 – 2008	Associate Editor IEEE Transactions on Neural Networks	IEEE
2005 –	Task Force on Nano Architectures	IEEE-CS
2003 –	Member of the Novel Nanoarchitectures Study Group CW4	SRC-NNI

Reviews

2016	[ongoing]					3 journals	22 conferences
2015						8 journals	42 conferences
2014	1 NSF					30 journals	45 conferences
2013	1 NSF					31 journals	58 conferences
2012					2 MSc	33 journals	46 conferences
2011	1 NSF	2 EU				19 journals	31 conferences
2010		1 EU		1 Cyprus		14 journals	24 conferences
2009		1 EU	1 Belgium	1 Cyprus	1 PhD	13 journals	25 conferences
2008	1 NSF	1 EU	1 Switzerland		4 PhDs	15 journals	33 conferences
2007	1 NSF	1 EU		1 book	1 PhD	9 journals	28 conferences
2006	1 NSF		1 Switzerland	2 books	1 PhD	15 journals	15 conferences
2005	1 NSF		1 Belgium	1 book	1 PhD	5 journals	11 conferences

[…]

Honours and Awards

3 Visiting

2016	Erasmus Mundus (Visiting Prof.)	European Union (hosted by TU Dresden / CfAED)	2 months
2013	Erasmus Mundus (Nano Scholar)	European Union (hosted by TU Dresden / CfAED)	1 month
2005 – 2011	Visiting Professor	Ulster University (UK)	

5 Felloswhips

1999 – 2001	Rose Research Fellowship	Rose Research (USA)	0.1%
1996 – 1998	Director's Postdoctoral Fellowship	Los Alamos National Laboratory (USA)	1.0%
1994 – 1996	HCM Research Fellowship	European Union (King's College London, UK)	0.1%
1993 – 1994	Research Fellowship	Concerted Research Action (Flemish Community)	
1991	Fulbright Fellowship	Fulbright Commission (USA)	0.1%

2 Scholarships

1991 – 1993	Doctoral Scholarship	Katholieke Universiteit Leuven (Belgium)	1.0%
1975 – 1980	National Merit Scholarship	Ministry of Science & Education (Romania)	0.1%

Others

2009	Research Affairs Recognition Award	UAEU	1.0%
2009	Best Excellence in Scholarship Award	UAEU, College of IT	2.0%
2008	Best Paper Award	UAEU Annual Research Conference	1.0%
2003	Two Patents	US PTO (2)	
2002	Six Patents	US PTO (3), Taiwan PTO (3)	
2001	US resident under extraordinary ability	"VLSI implementations of neural networks"	
2001	Two Patents	US PTO (2)	
2000	Best Paper Award	IEEE CAS'2000	1.0%
1996	Senior Member	IEEE	8.0%
1994	PhD summa cum laude	Katholieke Universiteit Leuven (Belgium)	
1984	One Patent	Romanian PTO (1)	
1980	Best MSc Thesis Award	University "Politehnica" of Bucharest (Romania)	1.0%
1980	Best Paper Awards (three times)	University "Politehnica" of Bucharest (Romania)	1.0%
1977	Best Paper Awards (two times)	University "Politehnica" of Bucharest (Romania)	1.0%
1975	Highest Award (at graduation)	National College of Informatics (Romania)	0.1%
1971 – 1975	Gold Medal/First Prize (four times)	Romanian Physics Olympiad	0.1%

Memberships

IEEE	Institute of Electrical and Electronic Engineers IEEE (1992) **Senior Member** since 1996
INNS	International Neural Network Society (since 1992)
ENNS	European Neural Network Society (since 1991, founding member)
ACM	Association for Computing Machinery (1999)
MCFA	EU Marie Curie Fellowship Association (since 1999)
CIRU	Centre International de Rencontres Universitaire / Lions Club International (since 1999)

1267 citations Excluding self-citations (hand counted; available upon request) **246 publications**

Citation analysis (as of May 28, 2016)		# publications	h
391/254	Web of Science (including / excluding self-citations)	117	9
739	Scopus (including self-citations) http://www.scopus.com/authid/detail.url?authorId=7004865225	135	13
760	Semantic Scholar (including self-citations) https://www.semanticscholar.org/author/Valeriu-Beiu/1695884		
2029	Google Scholar (including self-citations) http://scholar.google.com/citations?user=5dqCk98AAAAJ&hl=en	246	22
2033	Publish or Perish (including self-citations)	292	21

ANNEXES

Links related to vita

1971 – 1975	"Tudor Vianu" National College of Informatics	http://www.lbi.ro/
1975 – 1980	University "Politehnica" of Bucharest	http://www.upb.ro/en/
	Faculty of Control & Computers	http://acs.pub.ro/en/
	CS&E Department	https://cs.pub.ro/
	MSc supervisor	http://ro.wikipedia.org/wiki/Mircea_Petrescu
1980 – 1982	Research Institute for Computer Techniques	http://www.itc.ro/
1982 – 2001	University "Politehnica" of Bucharest	http://www.upb.ro/en/
	Faculty of Control & Computers	http://acs.pub.ro/en/
	CS&E Department	https://cs.pub.ro/
1991 – 1994	Katholieke Universiteit Leuven	http://www.kuleuven.be/english
	Faculty of Engineering	http://eng.kuleuven.be/
	EE Department (ESAT)	http://www.esat.kuleuven.be/
	PhD supervisor	http://www.esat.kuleuven.be/stadius/person.php?persid=18
1994 – 1996	EU HCM Fellowship	http://cordis.europa.eu/tmr/src/grants/chbi/chbig_ro.htm
	King's College London	http://www.kcl.ac.uk/
	School of Natural & Mathematical Sciences	http://www.kcl.ac.uk/nms/
	Department of Mathematics	http://www.kcl.ac.uk/nms/depts/mathematics/
	Centre for Neural Networks	http://www.mth.kcl.ac.uk/cnn/ [old; not active]
	Scientific advisor	http://en.wikipedia.org/wiki/John_G._Taylor
1996 – 1998	Los Alamos National Laboratory	http://www.lanl.gov/
	Nonproliferation & International Security	http://nis-www.lanl.gov/ [old; not active]
1998 – 2001	RN2R / Rose Research LLC	http://patents.justia.com/assignee/RN2RLLC.html
2001 – 2005	Washington State University	http://www.wsu.edu/
	School of EE&CS	http://school.eecs.wsu.edu/
2005 – 2011	University of Ulster	http://www.ulster.ac.uk/
	Intelligent System Research Centre	http://isrc.ulster.ac.uk/
2005 – 2015	United Arab Emirates University	http://www.uaeu.ac.ae/en/
	College of Information Technology	http://www.cit.uaeu.ac.ae/en/
2015 –	"Aurel Vlaicu" University of Arad	http://www.uav.ro/en/

Links to 4 invited presentations

2014 Bio-Inspired Designing with Arrays
CMOS Emerging Technology Research CMOSETR'14, Grenoble, France, July 8, 2014
http://books.google.ca/books?id=OL3aAwAAQBAJ&pg=PA102

2013 Why Biology Can and Silicon Can't
TUDresden, Germany, July 11, 2013
http://nano.tu-dresden.de/pages/seminar_636.html
http://nano.tu-dresden.de/pubs/slides_others/2013_07_11_Beiu.pdf

2010 Trustworthy Wings of the Mysterious Butterflies
International Nanotechnology Conference INC6, Grenoble, France, May 19, 2010
http://www.minatec.org/inc6/presentations/We1-1_Beiu.pdf

2010 On Brain Inspired Nano Interconnects (tutorial)
IEEE International Joint Conference on Neural Networks IJCNN'10, Barcelona, Spain, July 18, 2010
http://cis.ieee.org/cis-educational-repository/cis-video-collection/cis-video-library.html?vid=35056547
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